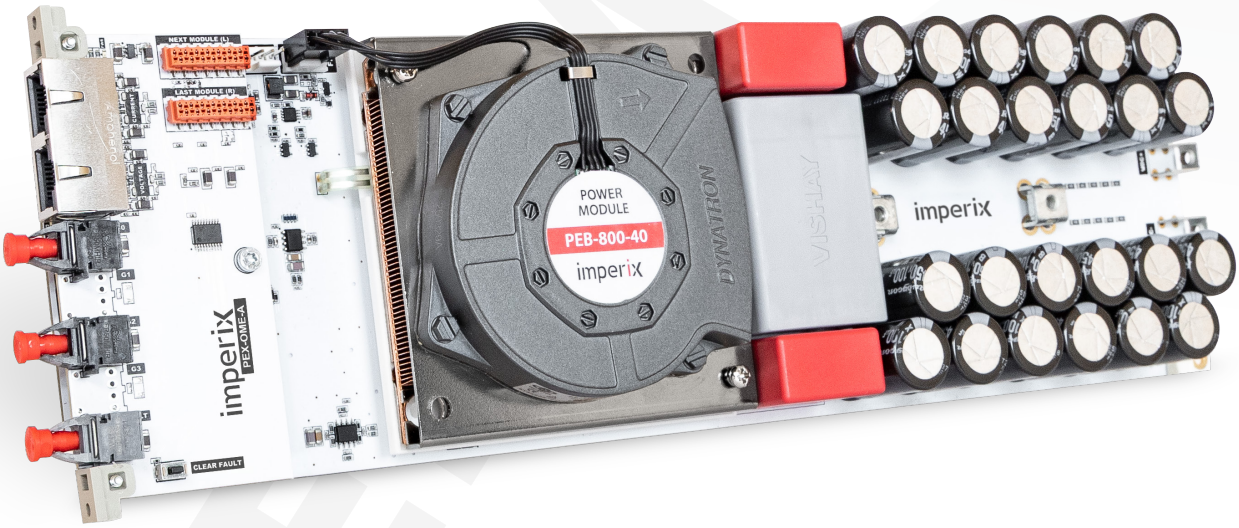
PEB-800-40

800V / 40A HALF-BRIDGE POWER MODULE



A TURNKEY BUILDING BLOCK
FOR POWER CONVERTERS

imperix

A versatile building block to implement most common converter topologies with little effort

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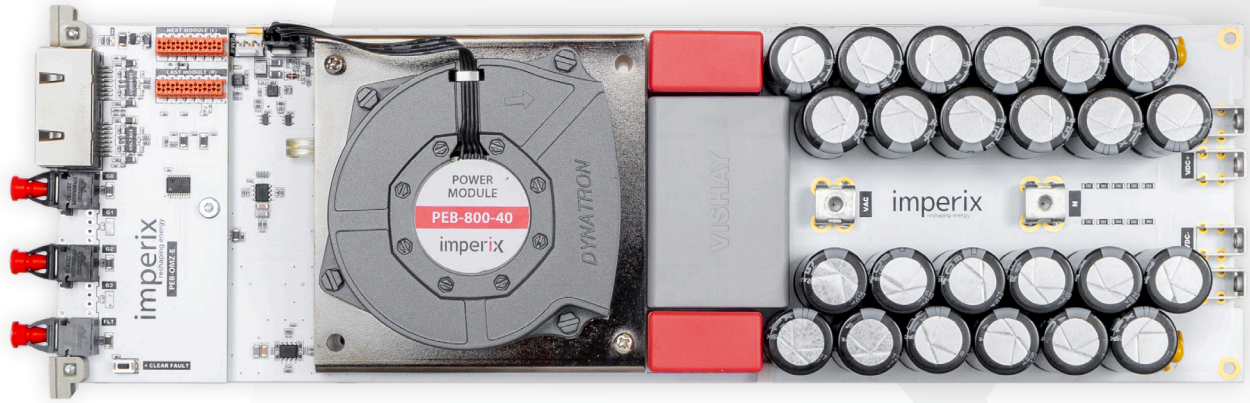


GENERAL DESCRIPTION

PEB-800-40 power modules are ready-to-use power electronic building blocks suitable for the implementation of power converters of a broad range of topologies. Built around a half-bridge switching cell made of two SiC semiconductors, the modules also embed all the necessary features to truly support the rapid implementation of laboratory prototypes, such as cooling, measurement, protection and discharge circuits.

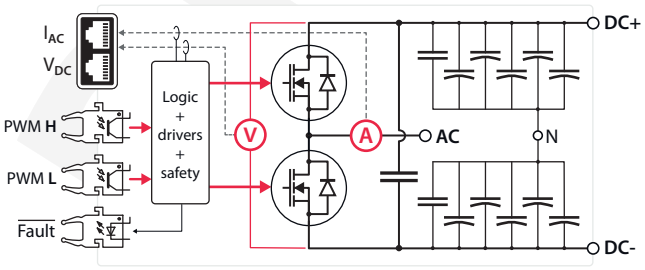
Leveraging two 1200V MOSFETs, the modules support up to 40 ARMS at 20 kHz or up to 200 kHz switching with reduced ratings, which typically enables the implementation of power converters from a few kW to hundreds of kW.

PEB-800-40 modules offer plug-&-play compatibility with imperix B-Box controllers, thanks to optical fiber inputs for the PWM signals, and ±5V analog signaling for the measurement outputs (over standard imperix RJ45 cables). Together, these products enable the implementation of most standard converter topologies in generally less than an hour.

KEY FEATURES AND SPECIFICATIONS

- Half-bridge topology with SiC MOSFETs
- 800 V nominal DC bus voltage
- 40 A continuous RMS current at 20 kHz
- Up to 200% overload capability for 500 ms
- Up to 200 kHz switching frequency
- Stackable DC buses up to 1.6 kVDC (two modules)
- Onboard DC voltage and AC current sensors
- Over-voltage / current / temperature protections
- Embedded 600 µF DC bus capacitance
- Variable-speed cooling (150W TDP)
- Sensor auto-configuration with B-Box 4 (1-wire link)

SIMPLIFIED SCHEMATIC



PRODUCT POSITIONING

Imperix modules distinguish from semiconductor modules (packages) and conventional power stacks as they offer a truly complete and ready-to-use power stage in a modularized building block. Control remains however to be implemented externally, e.g. using B-Box 4.

PEB-800-40 modules supersede and replace the previous-generation PEB8038 and PEB8024 modules, thanks to superior power ratings over the whole range of operating conditions.

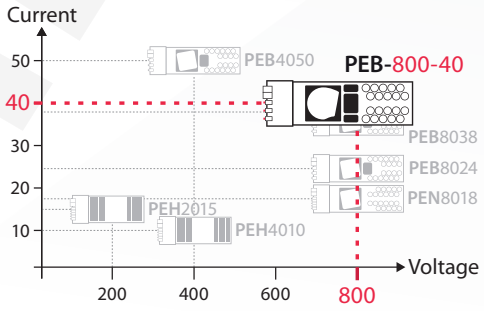


Fig. 1. Ratings of the PEB-800-40 compared to other imperix modules

PEB-800-40 also offer superior mechanical construction, superior AC current and DC voltage sensors, improved galvanic isolation, as well as protection against DC midpoint imbalance. Furthermore, the new modules now implement smart protection thresholds, which are computed in real time as a function of the DC bus voltage, average duty cycle and switching frequency, following an I2t characteristic. This allows for a doubled short-term current rating when compared to the long-term tolerable value.

SIMILAR PRODUCTS

Previous modules remain available for sale, notably for supporting the extension of existing systems with maximum compatibility. Besides, IGBT-based modules featuring other cells topologies may also constitute attractive alternatives for specific applications.

Module	Type	Voltage	Current	Frequency	Production
PEB-800-40	Half-bridge	800 V_{DC}	40 A_{RMS}	1-200 kHz	Active
PEH 2015	Full-bridge	200 V_{DC}	15 A_{RMS}	1-20 kHz	Active
PEH 4010	Full-bridge	400 V_{DC}	10 A_{RMS}	1-20 kHz	Active
PEN 8018	NPC phase-leg	800 V_{DC}	18 A_{RMS}	1-20 kHz	Active
PEB 4050	Half-bridge	800 V_{DC}	50 A_{RMS}	1-20 kHz	NRND
PEB 8024	Half-bridge	800 V_{DC}	24 A_{RMS}	1-200 kHz	NRND
PEB 8038	Half-bridge	800 V_{DC}	38 A_{RMS}	1-20 kHz	NRND

EXAMPLE OF USE

An elementary use case of the PEB-800-40 is shown in Fig. 2, which implements the module in a buck configuration, hence producing a controllable switched voltage thanks to suitable PWM signals. If desired, feedback control can be rapidly implemented and tested, for instance to optimize the stability or dynamic performance of a control technique, such as for the output current, voltage or power.

In this case, several products are employed alongside the module:

- A so-called type A mounting system
- A fully-programmable digital controller, here the B-Box 4
- External current and/voltage sensors
- Passive components, such as inductors or filters
- Power sources and loads (e.g. DC power supply and resistors)

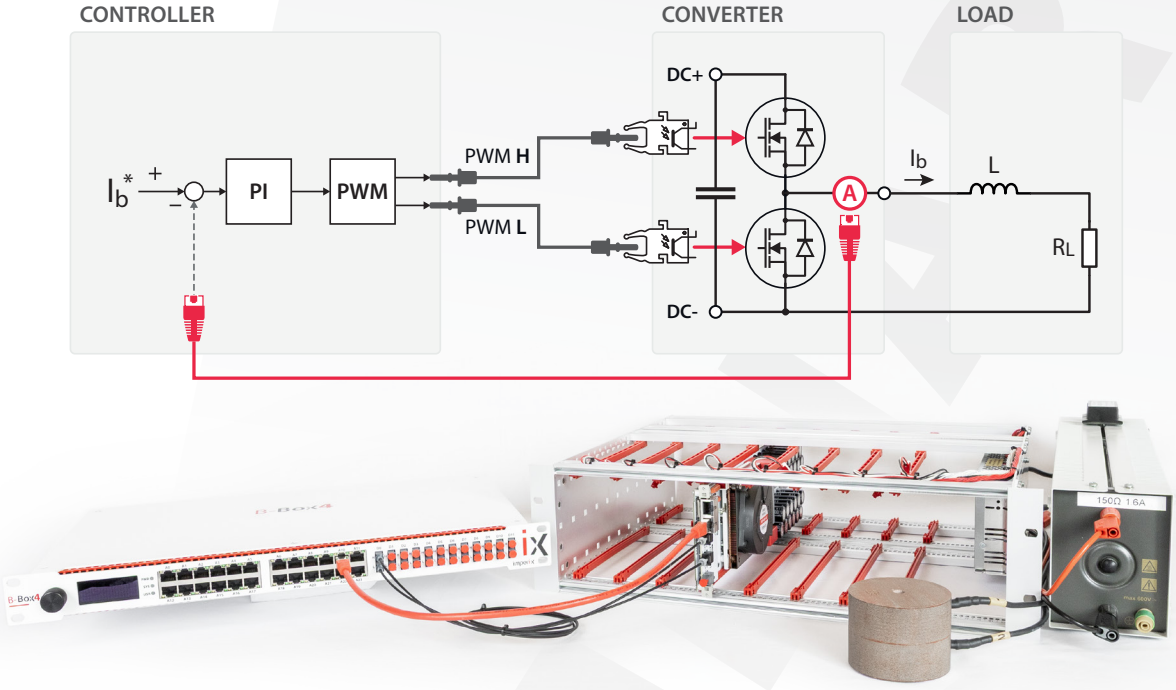


Fig. 2. Example with a B-Box 4 used to control a PEB-800-40 implemented as a buck converter.

POWER CIRCUIT

PRINCIPLE OF OPERATION

Each power transistor (Infineon IMZA120R014M1HXKSA1) is directly driven by the corresponding optical receiver. In-between, only a logic inverter and the FPGA are present, adding minimum skew and delay.

In case of any fault (see "fault conditions" on page 8), both signals are instantly blocked by the FPGA. Simultaneously, the **nFault** signal is also turned low – dark on the fault feedback emitter – to signal the fault. Further details on these mechanisms are given in the section "Embedded logic and protection" on page 8.

The optical receivers are compatible with standard 650 nm Plastic Optical Fibers (POF) or Plastic Clad Silica (PCS) fibers. The FD-02M-BSB (Firecomms) is one example of a compatible POF. No special coding is required: light 'ON' applies a positive voltage on the gate; light 'OFF' applies a negative one.

A galvanic isolation is implemented between the power and logic circuits. Configurations with either a floating DC bus or a grounded DC+ or DC- terminal are possible. Stacked DC busses are also possible, hence potentially reaching a total of 1600V (±800VDC) with suitable enclosures and cabling.

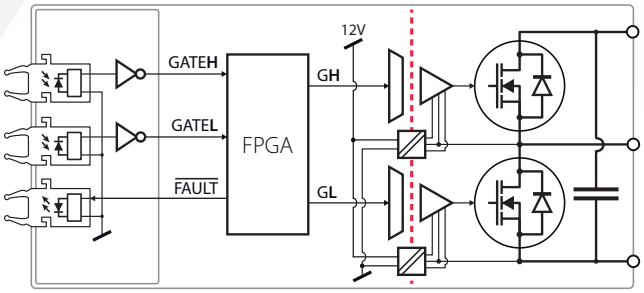


Fig. 3. Functional schematic of the power stage.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Maximum DC bus voltage [1]	$V_{DC,max}$	Power module not switching	–	900	–	V
Maximum DC bus ripple current [2]	I_{ripple}	f = 120 Hz	–	9	–	A_{RMS}
		f = 100 kHz	–	18	–	A_{RMS}
Maximum repetitive peak isolation voltage	V_{IORM}	60s, AC	–	2.9	–	kV_{RMS}
Continuous total power dissipation	P_{cooler}		–	150	–	W
Operating ambient temperature	T_a		0	–	45	°C

POWER CHARACTERISTICS

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
DC bus voltage	V_{DC}		–	800	–	V
Continuous leg current [3]	I_{AC}	T_C = 100°C, f_{SW} = 20 kHz Reverse conduction in the channel [4]	–	40	–	A_{RMS}
Overload current capability	I_{OVL}	Referred to $I_{SOA}(f_{SW}, V_{DC}, d_{AVG})$, up to 500 ms	–	2	–	p.u.
DC bus capacitance	C_{DC}		–	600	–	µF
Drain-source on-state resistance	$R_{DS,on}$	V_{GS} = 15V , I_{DS} = 40 A, T_J= 25°C	–	17	–	mΩ
		V_{GS} = 15V , I_{DS} = 40 A, T_J= 175°C	–	30	–	mΩ
Diode forward voltage	V_F	I_{DS} = 40 A, T_J= 25°C	–	3.8	–	V
		I_{DS} = 40 A, T_J= 175°C	–	3.6	–	V
Voltage slope	dV/dt	Turn on, I_{AC} = 40 A_{RMS} , V_{DC} = 800 V	–	38	–	kV/µs
		Turn off, I_{AC} = 40 A_{RMS} , V_{DC} = 800 V	–	18	–	kV/µs
DC bus self-discharge time	$t_{discharge}$	From 800V to 50V, no external load	–	330	–	s

SIGNAL CHARACTERISTICS

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Gate voltage ON	G_H	fiber 'ON' (λ_R 635–680 nm, -22–2 dBm)	–	+15	–	V
Gate voltage OFF	G_L	fiber 'OFF' (< -40 dBm)	–	-5	–	V
Switching frequency	f_{SW}	Hard switching	–	20	200	kHz
Deadtime [5]	DT	V_{DC} = 800 V , I_{AC} = 6 A_{RMS}	120	–	–	ns
Propagation delay asymmetry (mezzanine)	T_2		–	–	9.5	ns
Propagation delay asymmetry (safeties + gate drivers)	T_3		–	–	22	ns
Propagation delay (mezzanine)			–	–	61	ns
Propagation delay (safeties + gate drivers)			–	–	137	ns
MOSFET turn-off time	$T_{d,off}$	V_{DC} = 800 V , I_{AC} = 40 A_{RMS}	–	17	–	ns
		V_{DC} = 800 V , I_{AC} = 6 A_{RMS}	–	39	–	ns
MOSFET fall time	T_r	V_{DC} = 800 V , I_{AC} = 40 A_{RMS}	–	27	–	ns
		V_{DC} = 800 V , I_{AC} = 6 A_{RMS}	–	41	–	ns
MOSFET turn-on time	$T_{d,on}$	V_{DC} = 800 V , I_{AC} = 40 A_{RMS}	–	56	–	ns
		V_{DC} = 800 V , I_{AC} = 6 A_{RMS}	–	48	–	ns
MOSFET rise time	T_f	V_{DC} = 800 V , I_{AC} = 40 A_{RMS}	–	45	–	ns
		V_{DC} = 800 V , I_{AC} = 6 A_{RMS}	–	105	–	ns

[1] The maximum DC bus voltage is defined by the specifications of the bus capacitors. Therefore, as for any aluminum electrolytic capacitors, few short-term over-voltages can be tolerated, provided that they involve limited amounts of energy.

[2] The maximum ripple current is defined by the equivalent series resistance (ESR) of the capacitors and relates to Joule losses and lifetime considerations. Therefore, this value can be temporarily exceeded, provided that the operating temperature of the capacitors remains low.

[3] In cold conditions, the maximum current is limited by the power semiconductors. Otherwise, the current rating of the module is limited by the power envelope of the cooler (about 150W with airflow).

[4] This indicates that both switches are actively used and that reverse conduction inside the MOSFET channel is used in order to reduce the conduction losses.

[5] The minimum recommended dead time was chosen conservatively. Please refer to PN115 at imperix.com/doc for more details.

LOSSES AND DERATING

The semiconductor losses are heavily dependent on the operating conditions. Therefore, due to a constrained power dissipation budget through the cooler (150W), derating may be required in special conditions. The corresponding derating curves define the so-called Safe Operating Area (SOA) and are represented in Fig. 4 – Fig. 6.

In the PEB-800-40, switching losses are dominant, exhibiting dependence on the DC bus voltage and the switching frequency. Current derating is therefore required above the nominal frequency. In some cases, this derating can be mitigated either by operating at a lower DC voltage, or by utilizing external components and circuit conditions to enable soft-switching (refer to established literature).

Conduction losses occur either in the $R_{DS,on}$ resistance of the MOSFETs or within the anti-parallel diodes. Therefore, depending on the employed modulation strategy and duty cycle, significant imbalance may occur between these components, and hence between the lower and upper switches. For this reason, current derating must also be applied whenever the average duty cycle deviates from 50% in order to avoid excessive temperature on one of the two switches.

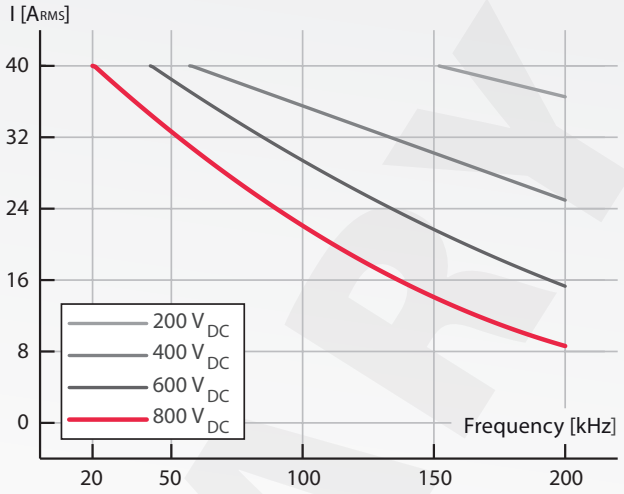


Fig. 5. Current capability as a function of the switching frequency.

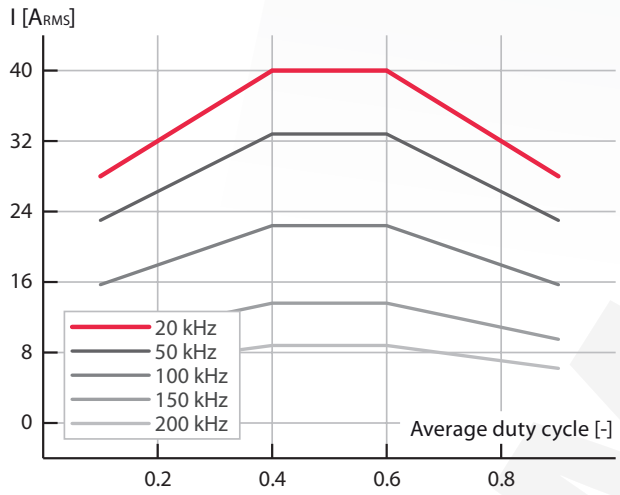


Fig. 4. Impact of semiconductor losses imbalance: current capability as a function of the average duty cycle.

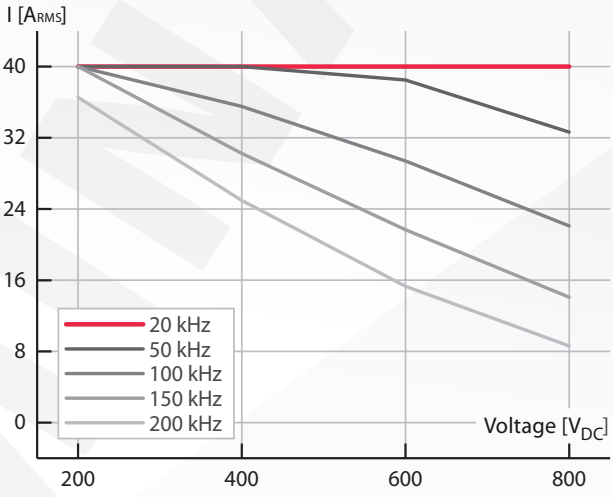


Fig. 6. Current capability as a function of the DC bus voltage.

NOTE:

The module's long-term performance ratings are detailed in Figures 4 through 6. The unit is also capable of accommodating short-term overloads, up to twice the long-term capability, for a maximum duration of 500 ms (refer to Figure 16). Both the Safe Operating Area (SOA) and the overload capability are enforced by the integrated protection logic, as detailed in the section "Embedded logic and protection" on page 8.

VOLTAGE SENSOR

PRINCIPLE OF OPERATION

The measurement of the DC voltage is implemented using precision resistive dividers on the two individual half-busses. Galvanic isolation is implemented using precision isolated amplifiers. The two corresponding measurements are subsequently combined by an operational amplifier, yielding a signal proportional to the total DC bus.

The voltage measurement is compatible with sensor auto-identification when using the B-Box 4. The associated pinout is given in Fig. 11.

Over-voltage protection is implemented by spying on the measurements of the individual DC busses, so that both the total DC bus as well as individual busses can be protected.

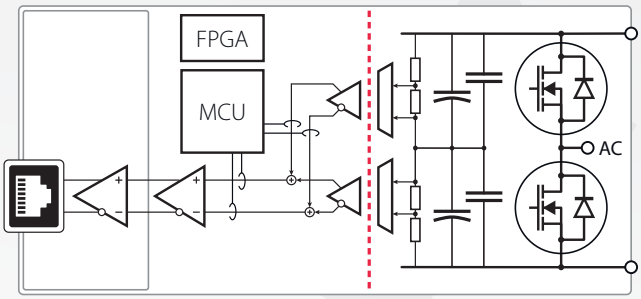


Fig. 7. Functional schematic of the DC voltage sensing circuit.

VOLTAGE SENSOR CHARACTERISTICS

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Nominal voltage, linear range	V_{NOM}		0	–	850	V_{pk}
Maximum measurable voltage	V_{MAX}		0	–	1000	V_{pk}
Nominal sensitivity	G	Including a x2 gain on the mezzanine board	–	5	–	mV/V
Sensitivity error	G_E		–	–	1.3	%
Input-referred offset	I_O	Disregarding EEPROM data	–	–	±200	mV
Measurement bandwidth	f_{3dB}		–	10	–	kHz
Input-referred noise	V_{noise}	Over the full BW	–	0.08	–	V_{RMS}
Over-voltage threshold, half DC bus		Onboard microcontroller	–	450	–	V
Over-voltage detection delay		Onboard microcontroller	–	< 50	–	µs

CURRENT SENSOR

PRINCIPLE OF OPERATION

The measurement of the output current (AC midpoint) is implemented using a high-precision shunt together with a precision isolated amplifier.

The current measurement is compatible with sensor auto-identification when using the B-Box 4. The associated pinout is given in Fig. 11.

Over-current protection is implemented by spying on the measurements and comparing its value with suitable protection thresholds, which are computed in real time by the micro-controller. Further details on this aspect are given in the section "Over-current protection" on page 9.

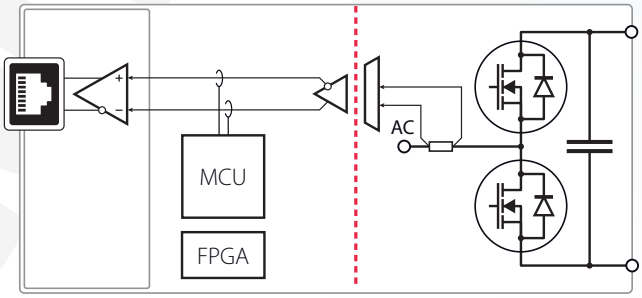


Fig. 8. Functional schematic of the AC current sensing circuit.

CURRENT SENSOR CHARACTERISTICS

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Nominal current, linear range	I_{NOM}		–	±62	–	A_{pk}
Maximum measurable current	I_{MAX}		–	±89	–	A_{pk}
Nominal sensitivity	G	Including a x2 gain on the mezzanine board	–	50	–	mV/A
Sensitivity error	G_E		–	–	1.0	%
Input-referred offset	I_O	Disregarding EEPROM data	–	–	±80	mA
Measurement bandwidth	f_{3dB}		–	75	–	kHz
Group delay		20 kHz	–	3.1	–	µs
		50 kHz	–	4.3	–	µs
		100 kHz	–	5.0	–	µs
Input noise	V_{noise}		–	10	–	mA_{RMS}
Shunt resistance	R_{shunt}		1.99	2	2.01	mΩ
Over-current threshold		Computed dynamically. See "Embedded logic and protection" on page 8.				
Over-current detection delay		< 15 µs when I_{AC} exceeds the overload capability curve (see Fig. 16)				

RIPPLE CURRENT TRACKING

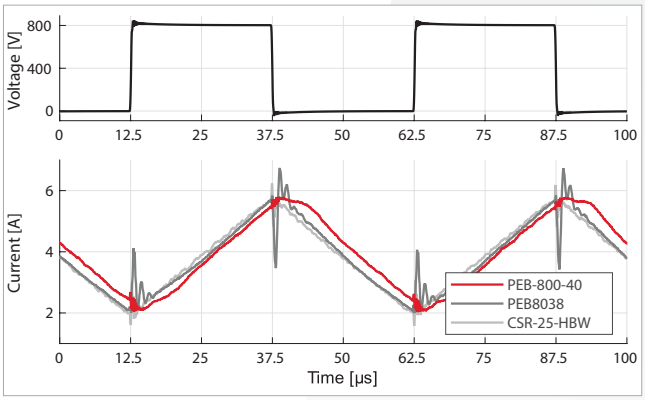


Fig. 9. Current tracking performance of the PEB-800-40 embedded sensor compared to other imperix products. $F_{SW} = 20$ kHz.

TRANSIENT VOLTAGE REJECTION

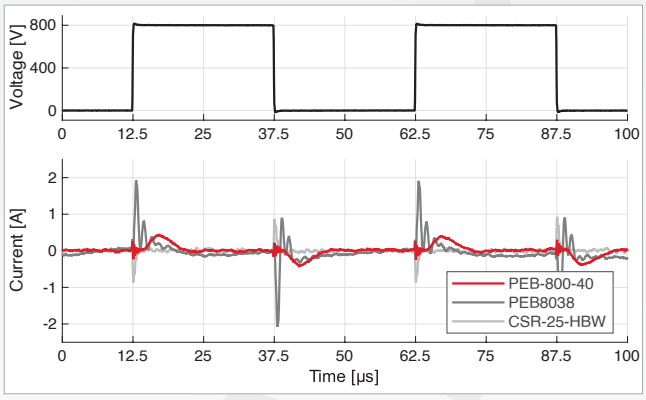
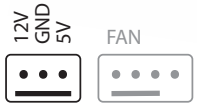


Fig. 10. Switch node voltage rejection of the PEB-800-40 compared to other imperix products.

POWER SUPPLY REQUIREMENTS

MAIN POWER SUPPLIES

The module requires 5V and 12V power supply voltages, which must be provided on a MTA100 three-position header (640454-3 from TE Connectivity), designated X5 on Fig. 20. The mating part is 3-643813-3 from the same supplier. The associated pinout is indicated below.



ANALOG POWER SUPPLIES

The last stage of the measurement circuits require analog power supplies of typically ±15V that must be provided on suitable pins of the RJ45 connectors. These are usually conveniently supplied directly by the B-Box, so that no user action is necessary. However, when the module is used with another controller, these pins cannot be left unconnected. The associated pinout is indicated below:

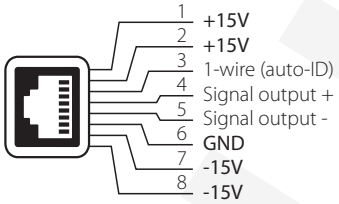


Fig. 11. Pinout of the RJ45 connectors used for analog signaling.

POWER SUPPLY CHARACTERISTICS

Parameter	Connector	Quantity	Min.	Typ.	Max.	Unit
+5V PSU	X5 (MTA100)	Voltage	4.7	5	5.3	V
		Power	–	1.1	1.4	W
+12V PSU		Voltage	10.8	12	13.2	V
		Power	–	9.8	13	W
±15V analog	P1 (2xRJ45)	Voltage	±12.5	±15	±17.5	V
		Power	–	0.1	1	W

Table 1. Required power supply specifications.

EMBEDDED LOGIC AND PROTECTION

PRINCIPLE OF OPERATION

The embedded protection logic operates as follows:

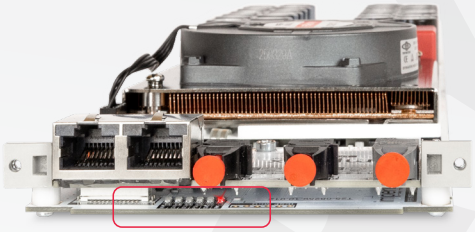
- A micro-controller (MCU) continuously samples selected analog quantities and evaluates them against fault conditions. Faults are immediately signaled to the FPGA by raising dedicated flags.
- A small FPGA implements combinatorial logic that regroups these flags, as well as triggers extra faults in special conditions (e.g. 1-1 condition on the PWM gating signals).

The overall logic is represented in Fig. 12. As shown, an active fault condition $\overline{\text{FAULT}}$='0' instantly blocks both PWM signals **GH** and **GL**, switches off the fault feedback optical emitter, and triggers the common **ERR_LINE** (see "Fault sharing and coordination" below).

FAULT SOURCE IDENTIFICATION

Six red LEDs are present on the front side of the module, under the mezzanine, indicating the origin of the fault, when applicable. The corresponding flags regroup the possible causes:

Flag	Description
VOLT	Over-voltage detected on the DC bus, or DC bus imbalance
CURR	Over-current detected at the switching node (AC)
COOL	Over-temperature on the cooler, or Probable fan fault (no tachometer signal)
P.SUP.	Inadequate power supply voltage
DESAT	Excessive drain-source voltage during on-state, or 1-1 condition detected on the provided PWM signals
RMT	Remote fault flag active (triggered remotely or locally)



FAULT CONDITIONS

The fault-triggering conditions are listed in the table below:

Event	Flag	Fault triggering when	Reaction time
Over-voltage	VOLT	$V_{DC} > 850$ V	< 50 µs
		$V_{DC,H}$ or $V_{DC,L} > 450$ V	< 50 µs
Over-current	CURR	$\lvert I_{AC}\rvert > 2 \times \lvert I_{SOA}(F_{SW}, V_{DC}, D_{AVG})\rvert$	< 15 µs
		$\lvert I_{AC}\rvert > \lvert I_{SOA}(F_{SW}, V_{DC}, D_{AVG})\rvert$	See overload capability
Cooling error	COOL	$T_{NTC} > 80$ °C	< 3 s
		Fan speed < 1000±200 rpm	< 5 s
Power supply error	P. SUP.	$V_{5V} < 4.5$ V or $V_{5V} > 5.5$ V	< 50 µs
		$V_{12V} < 11$ V or $V_{5V} > 13$ V	< 50 µs
MOSFET desaturation	DESAT	Excessive drain-source voltage during on-state or shoot-through	< 1.9 µs
1-1 gating signals		GATE_H = 1 and GATE_L = 1	< 20 ns
Remote fault	RMT	Triggered remotely or locally	< 20 ns

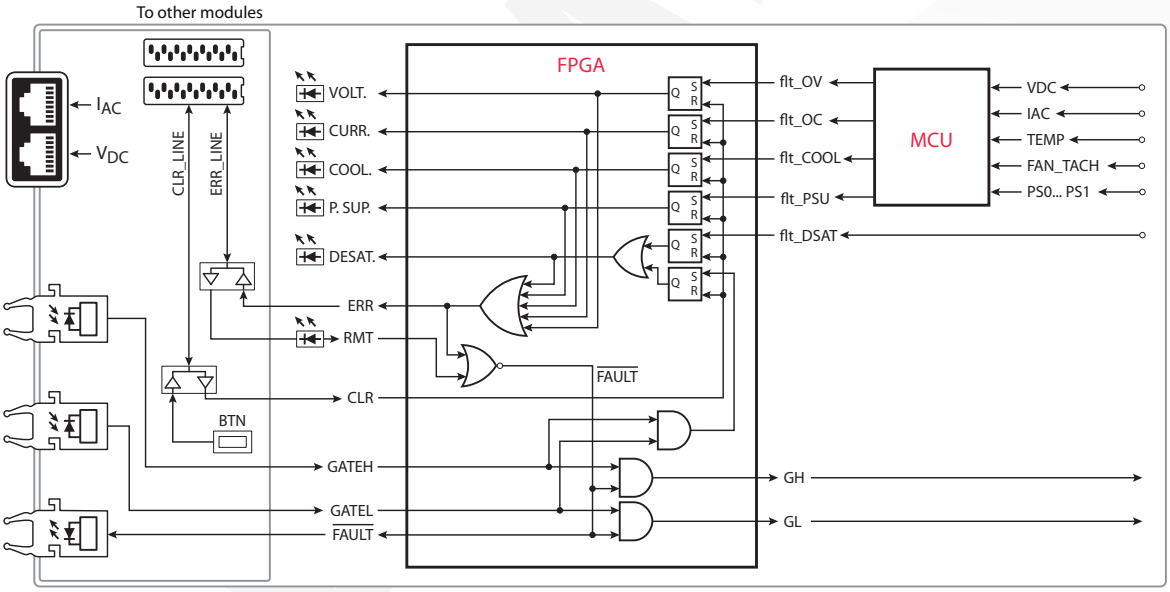


Fig. 12. Fault detection and protection logic.

FAULT SHARING AND COORDINATION

The optical fault feedback signal can be used for fault coordination, for instance using the optical expansion board for the B-Box 3/4. Alternatively, or additionally, fault conditions can also be shared across several modules by implementing a dedicated daisy chain (see Fig. 13). The corresponding cables are 2205065-1 from TE Connectivity. On a given module, the occurrence of an external fault is indicated by the RMT fault flag.

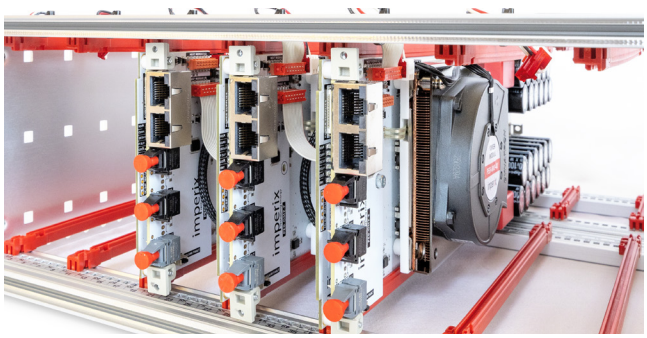


Fig. 13. Fault sharing using flat cables inside of a rack enclosure.

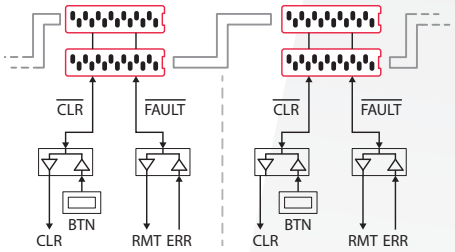


Fig. 14. Fault clearing and sharing. Simplified schematic.

FAULT ACKNOWLEDGMENT AND CLEARING

Fault flags are latched by the FPGA until the "CLEAR FAULT" button present on the mezzanine is pressed. After pressing the button, all fault status LEDs shall switch off, provided that the fault condition has disappeared in the meantime.

When implementing the daisy chain, an additional **CLR** signal is also shared across modules, so that the fault clearing can be centralized. Notably, in closed racks, a clear/reset button is available under the LCD screen for that purpose.

OVER-VOLTAGE PROTECTION

Over-voltage detection is implemented to guarantee that the maximum voltage ratings of the module are never exceeded, namely:

- The total DC bus voltage should not exceed 850V
- The individual half DC busses should not exceed 450V

If either of these thresholds is met, the flag **flt_OV** is raised.

These thresholds are constant and cannot be changed. Nonetheless, more restrictive thresholds can always be configured on the B-Box.

OVER-CURRENT PROTECTION

Over-current detection aims to prevent semiconductors from excessive heating, while maximizing the power transfer capabilities of the module given the operating conditions. To this end, the microcontroller dynamically computes the corresponding maximum tolerable long-term current (I_{SOA}) as a function of the operating point (F_{SW}, V_{DC}, d_{AVG}). Two protections thresholds are implemented according to the description made in Fig. 15:

- An instantaneous threshold (peak value) set at $2 \times I_{SOA}$.
- An I^2t protection set as a function of I_{SOA}, thereby allowing short-term overloads (see Fig. 16).

These thresholds are computed (interpolated) in real-time based on the derating curves. They cannot be changed. Nonetheless, more restrictive thresholds can always be configured on the B-Box.

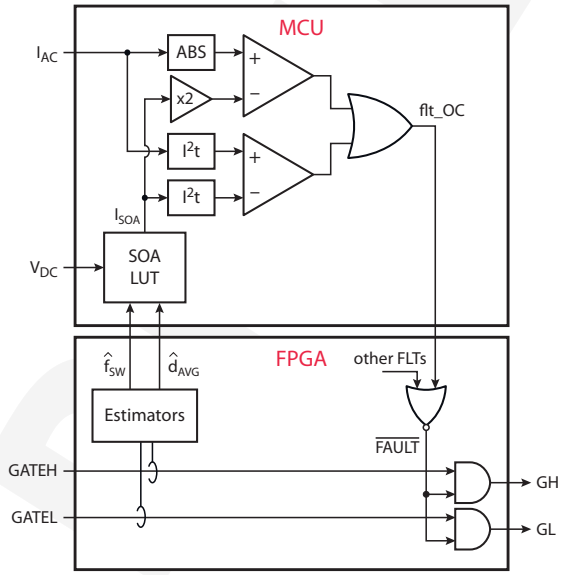


Fig. 15. Implementation of the over-current detection.

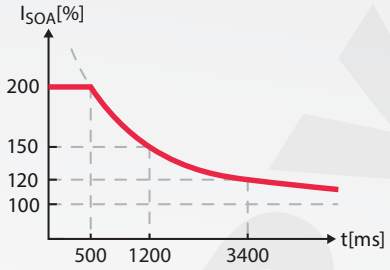


Fig. 16. Short-term current overload capability.

OVER-TEMPERATURE PROTECTION

Over-temperature detection aims to prevent damage to the MOSFETs due to excessive heating. To this end, the temperature of the semiconductors is indirectly measured using an NTC thermistor located on an aluminum plate, common to both switches (see Fig. 17).

THERMAL MODELING

A steady-state thermal model of the power module is presented in Fig. 18, where T_a designates the air temperature around the cooler (which may be inside an enclosure), T_{j1} and T_{j2} are the junction temperature of the two MOSFETs, and T_{NTC} represents the temperature of the aluminum plate. The corresponding thermal resistance are indicated in the table below.

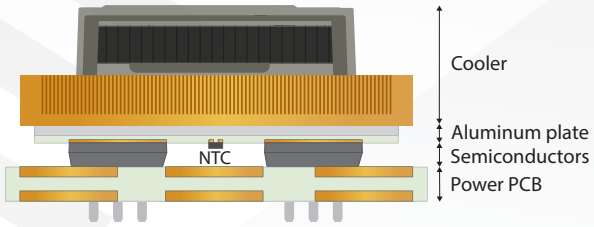


Fig. 17. Cross-section view of the power module (not up to scale).

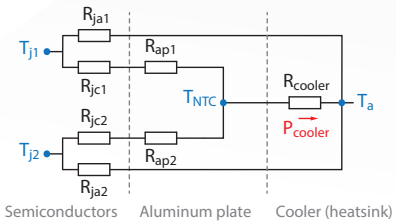


Fig. 18. Thermal model of the power module (steady-state).

Name	Description	Value	Unit
T_{j1} T_{j2}	MOSFETs junction temperature	–	°C
T_{NTC}	NTC temperature	–	°C
T_a	Cooling air temperature	–	°C
R_{jc}	Thermal resistance junction-to-case	0.33	°C/W
R_{ja}	Thermal resistance junction-to-air (MOSFET)	62	°C/W
R_{ap}	Thermal resistance case-to-aluminum plate	0.41	°C/W
R_{cooler}	Thermal resistance aluminum plate-to-air	0.28	°C/W

THERMAL PROTECTION

Thanks to the thermal model, the temperature of the semiconductors can be correlated to that of the NTC resistor. In practice, the implemented protection threshold is set at 80°C, which corresponds to a junction temperature of 150°C with an air temperature of 45°C, in steady-state. If this condition is met, the flag **flt_COOL** is raised.

In case the air temperature is over 45°C, the amount of losses that can be extracted by the cooler is reduced according to Fig. 19, thereby imposing a reduction of the module electrical power as well.

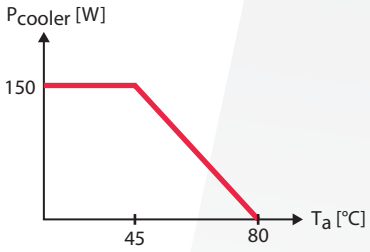


Fig. 19. Power dissipation derating with the ambient temperature.

ENVIRONMENTAL CONDITIONS

Parameter	Value
System voltage	850 V_{DC}, 291 V_{RMS}, OVC II, PD2
Operating conditions (IEC/EN 60721-3-3)	Climate conditions for operation class 3K3 : – Temperature range: 0°C to +40°C – Relative humidity: < 95%, no condensation – Atmospheric pressure: 70KPa to 106KPa
Storage conditions (IEC/EN 60721-3-1)	Climate conditions for storage class 1K3 : – Temperature range: -25°C to +55°C – Relative humidity: < 95%, no condensation – Atmospheric pressure: 70KPa to 106KPa

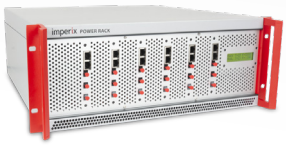
Table 2. Rated environmental conditions

ACCESSORIES

RACK INTEGRATION

The PEB-800-40 can be easily assembled within 19" rack-mountable enclosures. Two approaches are available:

- 3U open racks for handy and affordable integration
- 4U closed racks for sleeker and safer configurations, notably featuring safety laboratory plugs (banana) and an LCD screen.



EXTERNAL SENSORS

Imperix offers external current and voltage sensors, mountable on 35mm DIN rails. These may offer increased bandwidth and accuracy, or simply provide access to measurements that are not otherwise accessible. A typical example is the AC mains voltage, which must generally be measured on the other side of a connection relay, guaranteeing grid synchronization before connection.

The recommended products are listed below along with their main characteristics :

Sensor	Type	Range	BW	CMTI	Production
VSR-500-HBW	Differential	±500 V_{pk}	3 MHz	very high	Active
VSR-1000-ISO	Isolated	±1000 V_{pk}	100 kHz	very high	Active
CSR-25-HBW	Isolated	±25 A_{rms}	1.5 MHz	very high	Active

CABLES

POWER CONNECTORS

All power connectors (X1 to X4 in Fig. 20) possess M4 threaded holes. It is recommended to use cable shoes and a wire section of 4-10 mm^2.

OPTICAL FIBERS

PWM signals must be provided using plastic optical fiber cables (POF) with simplex friction plugs. They are available on the website.

ANALOG CABLES

Onboard measurements (current and voltage) are accessible with any standard RJ45 cable. Cables are available on the website.

MEZZANINE TO MEZZANINE CABLE

The fault signal can be shared among several modules using a 14-pin flat cable. The recommended reference is TE Connectivity 2205065-1.

Table 3.

MECHANICAL SPECIFICATIONS

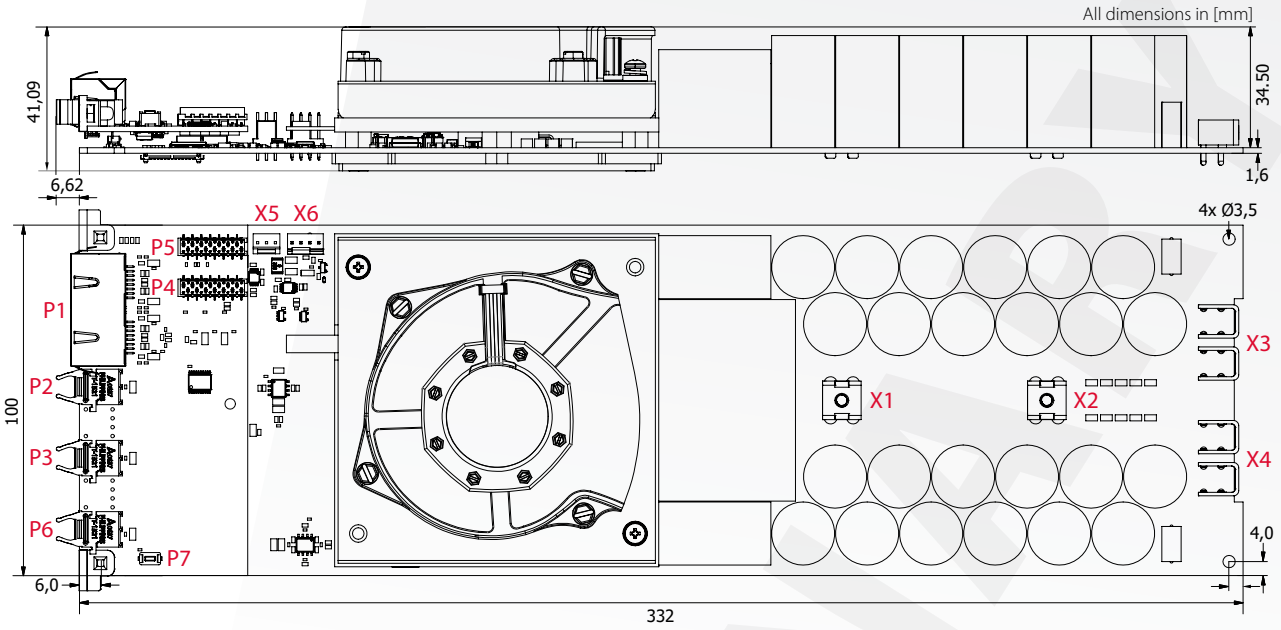


Fig. 20. Dimensional specifications of PEB modules

Label	Role
P1	RJ45 connector for measurements
P2	Gate H optical receiver
P3	Gate L optical receiver
P4	Mezzanine to controller connector
P5	Mezzanine to next mezzanine connector
P6	Global error optical emitter
P7	Clear fault button
X1	AC power terminal
X2	DC midpoint terminal
X3	DC+ power terminal
X4	DC- power terminal
X5	Auxiliary 5V+12V power supply connector
X6	Fan connector

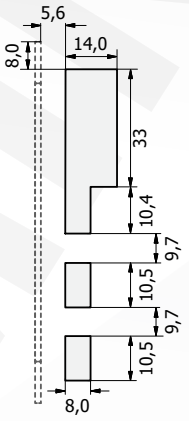


Fig. 21. Recommended front panel cut out

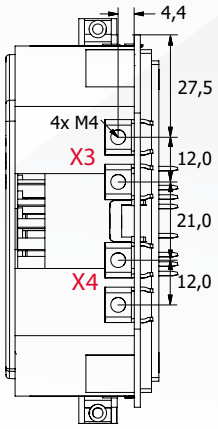


Fig. 22. DC bus power terminals

Caution, high risk of electrical shock!
All conducting parts must be inaccessible after installation.
When using the devices, certain parts may carry hazardous voltages (e.g. power supplies, busbars, etc.).
Power electronic modules must be used in electric / electronic installations with respect to applicable standards and safety requirements.
User must operate the devices in accordance with the manufacturer's operating instructions.
Disregarding this warning may lead to severe injury and/or cause serious damage.

REVISION HISTORY

- 15.12.25 : Preliminary version

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ABOUT US

Imperix develops high-end control equipment and prototyping hardware for power electronics, motor drives, smart grids and related topics. Our products are designed to accelerate the implementation of laboratory-scale power converters and facilitate the derivation of high-quality experimental results.

NOTE

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