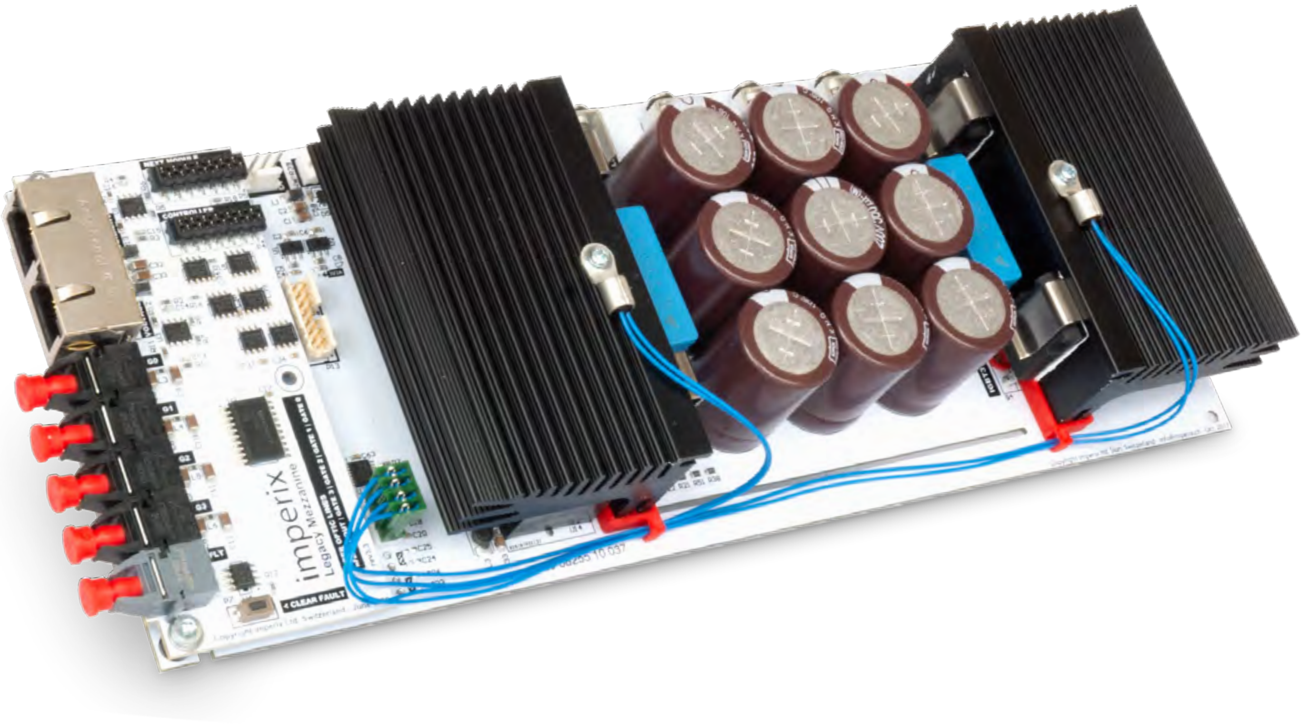
Rev. D / March, 2023



GENERAL DESCRIPTION

PEH modules are designed for the low-voltage laboratory implementation of multilevel converters. Configurable terminals allow to easily configure the modules for both half- or full-bridge operation. The design is tailored for 19" rack integration, offering plug-&-play connectivity with imperix B-Box controllers.

Direct access to the gating signals is offered using optical fiber inputs, while embedded measurement circuits provide analog outputs related to the capacitor voltage and one output current using galvanically-isolated sensors.

The modules are well suited for any kind of PWM operation from 0 Hz to 50 kHz and current ratings up to 15 A. The main limitation being the power envelope of the heatsinks, which is limited to approximately 20 W with no airflow and about 30 W with a 1 m/s airflow.

Overvoltage, over-current and over-temperature protections are also integrated on the board for safer use in R&D applications.

TYPICAL APPLICATIONS

The modules are best suited for the implementation of low-voltage prototypes of multilevel converters such as Modular Multilevel Converters (MMC), SSTs, cascaded H-bridge systems (CHB) or similar topologies. They can also be easily combined to build up simple DC-DC converters, Dual-Active Bridges (DAB), resonant converters, back-to-back systems, etc.

KEY FEATURES AND SPECIFICATIONS

- 15 A / 200 V maximum ratings, limited by losses
- 600 V / 50 A IGBTs
- 230 A maximum current (1 ms)
- 2 x 20 W TDP envelope
- Isolated TO247 transistor packages
- 5 mF / 200 V DC bus
- Up to 50 kHz switching frequency
- ±1.5 kV galvanic isolation (60s) / ±560 V (permanent)
- 4 optical PWM inputs / 1 optical FLT output
- Onboard voltage and current measurement
- Over-voltage/current/temperature protection

GENERAL SCHEMATIC

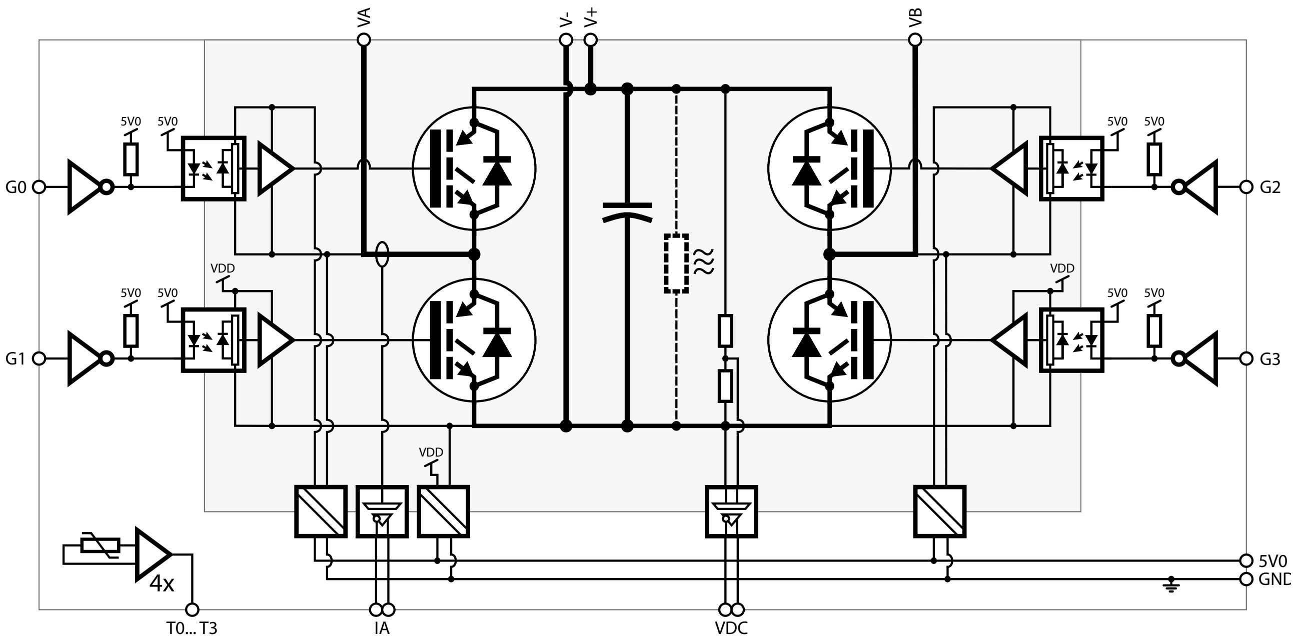


Fig. 1. Simplified schematic of the power stage of the H-bridge module. Embedded logic circuits and I/O connectors not shown.

MAIN COMPONENTS

Component	Devices	Main specifications
Power switches	*4x IXYS IXGR 48N60 C3D1*	*See below or device datasheet*
Capacitors	*9x Panasonic EET series 560 uF (total 5 mF)*	*200V, I_{RIPPLE} > 2.4A per capacitor (option)*
Drivers	*4x Avago HCPL-3140*	*0.4 A, 10 kV/us, V_{IORM} = 630V*
Isolated DC/DC Converters	*3x Recom RBM0515S*	*5-15 V, 1W, V_{IORM} = 1.1kV*
Current sensor	*1x Allegro ACS709-20*	*±37.5A, 120kHz, ±2% accuracy*
Voltage sensor	*1x Resistive divider + Texas Instruments AMC1200*	*60kHz, ±0.5% accuracy*
Heatsinks	*2x Fischer SK 487/84*	*84 x 52.3 x 28 mm, 2.5 K/W without airflow*
CPLD	*1x Xilinx XC9536XL-10VQG44C*	*10ns, 36 macrocells*
Microcontrollers	*2x Microchip PIC24F04KA201*	*16bits, 16Mhz, 9x 10-bit ADC @ 500ksps*

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Maximum DC bus voltage [1]	V_{DC}		-	200	-	V
Maximum continuous leg A / leg B current [2]	$I_{A/B,max}$	$T_J = 25°C$		56		A
Maximum DC bus ripple current (at 100 Hz) [3]	I_{RIPPLE}		-	21	-	A
Maximum working isolation voltage	V_{IORM}		-	560	-	V_{PK}
Highest allowable isolation voltage	V_{IOTM}	*60s isolation test*	-	1.5	-	kV_{PK}
Supply voltage	5V		4.2	5.0	5.8	V
Highest allowable junction temperature	$T_{J(max)}$		-	150	-	°C

[1] The maximum DC bus voltage is defined by the specifications of the bus capacitors. Therefore, as for any other aluminium electrolytic capacitors, few short-term overvoltages can be tolerated as long as they involve limited amounts of energy.

[3] The maximum ripple current is defined by the equivalent series resistance (ESR) of the capacitors and relates to Joule losses and lifetime considerations. Therefore, this value can be exceeded, provided that the operating temperature of the capacitors remain low.

[2] In cold conditions, the maximum operating current is limited by the power semiconductors. Otherwise, the current rating of the module is set by the power envelope of the heatsinks (about 20 W without airflow). This typically limits the RMS value of the phase-leg current to about 15 A for a switching frequency of 10 kHz.

POWER CHARACTERISTICS

Parameter	Symbol		Min.	Typ.	Max.	Unit
IGBT blocking voltage	I_{CES}	$T_J = 25$ to 150°C	-	600	-	V
IGBT continuous collector/diode current	I_{C25}	$T_J = 25$°C	-	56	-	A
	I_{C110}	$T_J = 110$°C	-	26	-	A
IGBT pulse collector/diode current (1 ms)	I_{CM}	$T_J = 25$°C	-	230	-	A
IGBT saturation voltage	$V_{CE(sat)}$	$I_C = 15$A, $T_J = 25$°C	-	2.1	-	V
		$I_C = 15$A, $T_J = 125$°C	-	1.3	-	V
Diode forward voltage	V_F	$I_F = 15$A, $T_J = 25$°C, $V_{GE} = 0$V	-	2.2	-	V
		$I_F = 15$A, $T_J = 125$°C, $V_{GE} = 0$V	-	1.5	-	V
Reverse recovery current	I_{RRM}	$I_F = 30$A, $V_R = 100$V, di/dt = -100A/µs	-	4	-	A
Reverse recovery delay	t_{RR}	$I_F = 1$A, $V_R = 30$V, di/dt = -100A/µs	-	100	-	ns
Thermal resistance junction-to-pad	R_{thJP}		-	-	1.5	°C/W
Thermal resistance heatsink-to-air	R_{thSA}		-	2.5	-	°C/W
Turn-on losses (inductive load)	E_{on}	$I_C = 15$A, $V_{CE} = 200$V, $T_J = 25$°C	-	150	-	µJ
		$I_C = 15$A, $V_{CE} = 200$V, $T_J = 125$°C	-	250	-	µJ
Turn-off losses (inductive load)	E_{off}	$I_C = 15$A, $V_{CE} = 200$V, $T_J = 25$°C	-	80	-	µJ
		$I_C = 15$A, $V_{CE} = 200$V, $T_J = 125$°C	-	130	-	µJ
Case-to-heasink isolation voltage	V_{ISO}	50Hz, 1min		2.5		kV

Assuming a phase-leg current of 15 A_{RMS} and a switching frequency of 10 kHz for each device, these characteristics lead for each phase-leg to approximately:

- conduction losses: 20 W hot / 35 W cold
- switching losses: 4.2 W hot / 2.7 W cold

The total thermal resistance junction-to-air is approximately 4.0 to 4.5°C/W, leading to a junction temperature of typically 120 to 130°C for the above-mentioned operating conditions and losses, assuming an ambient air temperature of 25°C.

CURRENT MEASUREMENT CHARACTERISTICS

Parameter	Symbol	Note	Min.	Typ.	Max.	Unit
Optimized accuracy range	I_{OPT}		-	±20	-	A
Linear range	I_{FS}		-	±37.5	-	A
Nominal sensitivity [4]	G	*Including a -2 gain on the mezzanine*	- 72.0	- 74.0	- 77.2	mV/A
Total output error [5]	G_{ERR}	$T_A = 25$°to 100 °C	-	±0.5	±2.0	%
Bandwidth	f_{3dB}		-	120	-	kHz
Measurable slope	dI/dt		-	6	-	A/µs
Maximum working isolation voltage	V_{IORM}		-	390	-	V_{DC}

VOLTAGE MEASUREMENTS CHARACTERISTICS

Parameter	Symbol	Note	Min.	Typ.	Max.	Unit
Measurement range	V_{OPT}		0.0	-	250	V
Maximum measurement range	V_{FS}		0.0	-	450	V
Nominal sensitivity [4]	G	*Including a -2 gain on the mezzanine*	-	- 8.9	-	mV/V
Uncalibrated sensitivity error [5]	G_{ERR}	*25°to 125 °C, including resistive divider*		±2.0		%
Gain error over temperature	$G_{ERR,t}$	$T_A = 25$°to 100 °C		±0.1		%
Bandwidth	f_{3dB}		-	25	-	kHz
Measurable slope	dV/dt		-	220	-	V/µs
Maximum working isolation voltage	V_{IORM}		-	1140	-	V_{DC}

[4] The negative value is due to the –2 inverting gain on the mezzanine. Current and voltage polarity is hence swapped.

[5] Superior performance can be achieved if calibrated under stable thermal conditions.

I/O MEZZANINE BOARD

The modules host a child mezzanine board providing optical inputs for PWM signals as well as analog outputs.

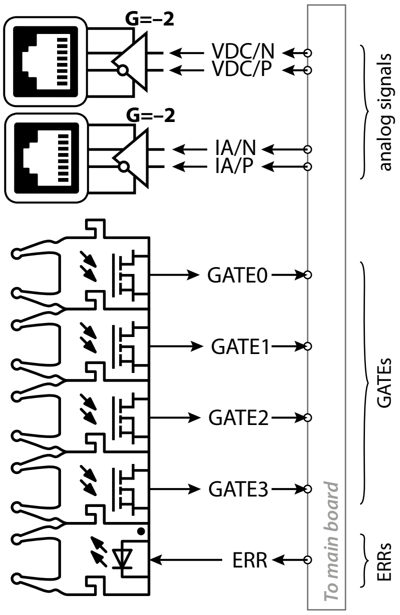


Fig. 2. Functional view of the mezzanine board.

ADDITIONAL FEATURES

Discharge resistor

An optional 10 kΩ / 10W resistor can be mounted on the module to provide a passive discharge mechanism. With an onboard capacitance of 5 mF, this results in a time constant of 50 s.

Connections

The power connections are located on top of the module, using M4 screw terminals, as shown in Fig. 4. This permits the easy reconfiguration of the topology, while guaranteeing robust mechanical contacts.

Temperature measurements

The modules embed 4 inputs for temperature sensors. Their simplified schematic is given in Fig. 3. These inputs are best suited with 5 to 50 kΩ NTC thermistors.

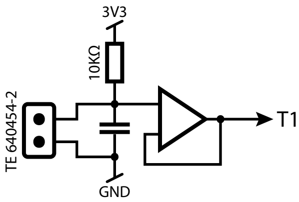


Fig. 3. Simplified schematic of one temperature input.

Eq. (1) and Eq. (2) describe the relationship between the measured temperature and the corresponding voltage. For the pre-mounted chips, $B = 3435\,K$ and $R_{25} = 10\,K\Omega$.

$$V_{T1} = \frac{R_{NTC}}{R_{NTC} + 10\text{K}} \cdot 3.3\text{V} \quad \text{Eq. (1)}$$

$$R_{NTC} = R_{25} \exp\left[B\left(\frac{1}{T} - \frac{1}{298.15}\right)\right] \quad \text{Eq. (2)}$$

Temperature limits are defined in the **MCU2** microcontroller, whose operation is described in the *embedded circuit logic and protection* section.

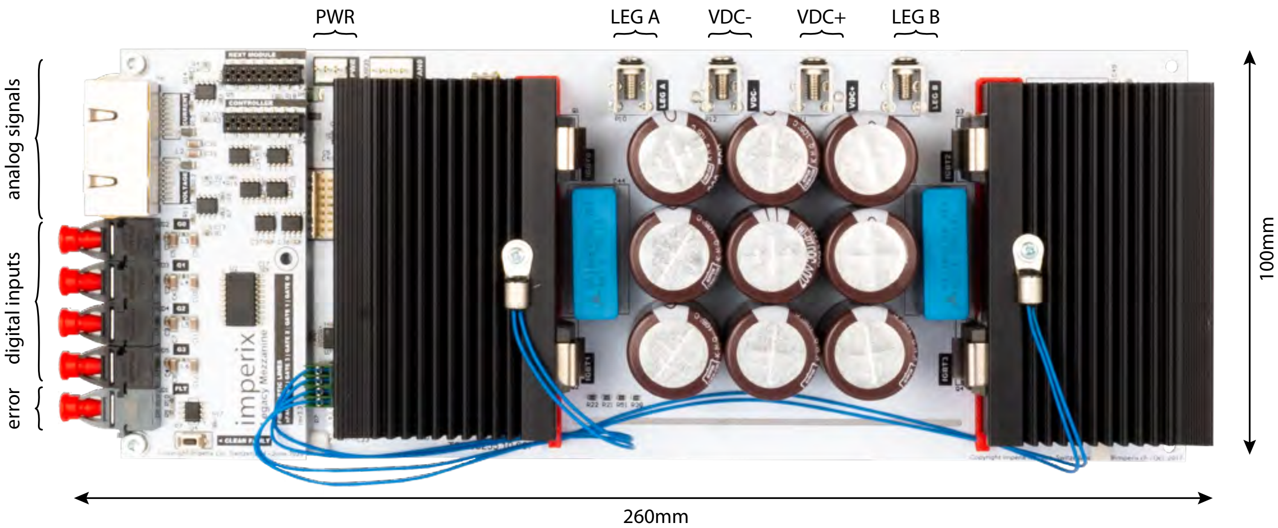


Fig. 4. Top view of the module with its main inputs / output connections.

EMBEDDED LOGIC AND PROTECTION

The modules embed a digital supervisory system that guarantees their integrity by a continuous monitoring of the measurements given by the voltage and current sensors, as well as the temperature probes and power supply voltage(s). The main components of this circuit are as follows :

» **MCU1** is continuously sampling the voltage and current at approximately 150 ksps. Upon the detection of an overvalue, the MCU triggers the corresponding flag.

» **MCU2** is continuously sampling slow variables such as temperatures, power supply voltage(s) or other measurements. Upon the detection of an overvalue, the MCU triggers the corresponding error flag.

» The **CPLD** is at the heart of the supervisory system and has three main tasks :

  » Generating the final gating signals based on those received through the optical fibers, possibly involving some decoding of the switching states.

  » Enforcing a specific switching state in case of a fault. This may be a blocked state or a short circuit depending on the desired behavior and the cause of the fault.

  » Generating a set of flags based on the faults provided by the microcontrollers.

Default configuration

The modules are provided with a default configuration implementing the following thresholds :

Signal name	Fault-triggering when
Cell output current	$\|I_A\| > 25\,A$
Capacitor bank voltage	$V_{DC} > 250\,V$
Heatsink temperature (1 and 2)	$T > 90°C$
5V power supply	$V_{sv} < 4.5\,V$ or $V_{sv} > 5.5\,V$

The global error signal transmitted by the mezzanine is turned off upon a fault detection (active low). When a faults is tripped, it can be cleared manually by pressing the corresponding button.

Fault status LEDs

Six red LEDs are present on the front side of the module, under the mezzanine, indicating the origin of the fault, when applicable. After pressing the clear button, all fault status LEDs shall switch off, provided that the fault condition has disappeared.

N°	Text	Description
1	*VOLT.*	*Over-voltage detected on the DC bus*
2	*CURR.*	*Over-current detected on the switching node (AC)*
3	*DESAT.*	*Unused on PEH modules*
4	*P. SUP.*	*Inadequate power supply voltage*
5	*T. FAN*	*Over-temperature on the cooler or fan fault*
6	*RMT*	*Unused on PEH modules*

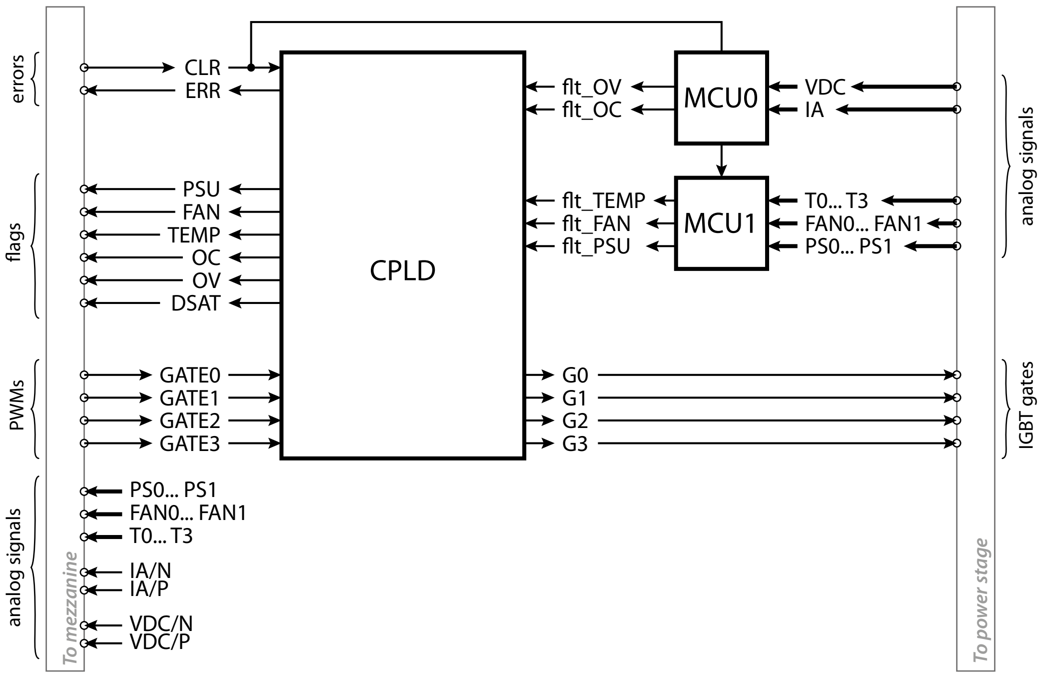
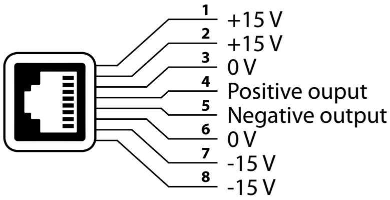


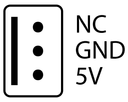
Fig. 5. Onboard protection and logic circuits.

ANALOG OUTPUT CONNECTORS PINOUT



POWER SUPPLY CONNECTOR

The pinout of the main power connector is as follows:



CABLES AND CONNECTORS

Power connectors

Power terminals (see Fig. 4) possess M4 threaded holes. It is recommended to use cable shoes and a wire section of at least 2.5 mm^2.

Optical fibers

PWM gating signals must be supplied using 650 nm POF cables with simplex friction plugs. They are available on the website.

Power supply connector

The power supply inlet uses of a 3-position MTA 100 terminal. A wire section of at least 0.25 mm^2 is recommended.

Analog cables

On-board measurements (current and voltage) are accessible using standard RJ45 cables. Cables are available on the website.

These modules must be used in electric / electronic equipment with respect to applicable standards and safety requirements in accordance with the manufacturer's operating instructions. Caution, risk of electrical shock! When using the devices, certain parts of the modules may carry hazardous voltages (e.g. power supplies, busbars, etc.). Disregarding this warning may lead to injury and / or cause serious damage. All conducting parts must be inaccessible after installation.

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ABOUT US

Imperix develops high-end control equipment and prototyping hardware for power electronics, motor drives, smart grids and related topics. Our products are designed to accelerate the implementation of laboratory-scale power converters and facilitate the derivation of high-quality experimental results.