TPI8032 22kW

All-in-one programmable inverter

The TPI8032 is an all-in-one three-phase inverter featuring imperix B-Board PRO programmable controller at its core.



GENERAL DESCRIPTION

The TPI8032 is an all-in-one three-phase inverter featuring imperix B-Board PRO programmable controller at its core. With its 22 kW power rating packed into a 1.5U 19" rack form factor, the TPI offers a high power density in a slim and compact chassis.

Unlike off-the-shelf industrial inverters, the TPI8032 is fully programmable and allows the implementation of advanced control techniques on both its DSP and FPGA. Thanks to its ultra-fast switching Silicon Carbide MOSFETs and its high-performance controller, the programmable inverter is particularly suited for demanding closed-loop methods requiring a high control bandwidth.

The power stage includes a comprehensive filtering solution to produce sinusoidal output voltages and currents and complies with the CISPR11 standard for electromagnetic compatibility. As an all-in-one solution, the TPI also embedds numerous voltage and current sensors, enabling a wide range of closed loop control methods.

Hardware protections against over-voltage, over-current, and over-temperature are built into the converter and operate independently from the main controller. For grid-tied applications, an AC pre-charge circuit ensures a safe connection to the grid.

Multiple units can operate together as a networked control system thanks to imperix *RealSync* proprietary technology. Combined with its compact design and high power density, the TPI8032 is perfectly suited for parallel operation.

TYPICAL APPLICATIONS

Considering its three-phase two-level inverter topology, the TPI8032 is meant for DC/AC microgrid applications at 230/400 VAC at 50Hz or 110/480 VAC at 60 Hz.

The automated precharge circuit simplifies the grid connection procedure while the filtering solution significantly improves the power quality factor. Typical applications include:

- Grid following inverters
- Grid forming inverters
- Active front ends
- Regenerative AC electronic loads
- Grid emulator

KEY FEATURES AND SPECIFICATIONS

- Three-phase two-level inverter topology (SiC MOSFETs)
- 800 V nominal DC bus voltage
- 32 A continuous RMS current at 50 kHz
- Up to 150 kHz switching frequency at 800 VDC
- 230/400 VAC at 50 Hz or 110/ 480VAC at 60 Hz operation
- LC and EMC filters
- On-board voltage and current sensors
- Over voltage/current/temperature protections
- Automated AC pre-charge circuit
- Fully programmable on-board controller

FRONT PANEL

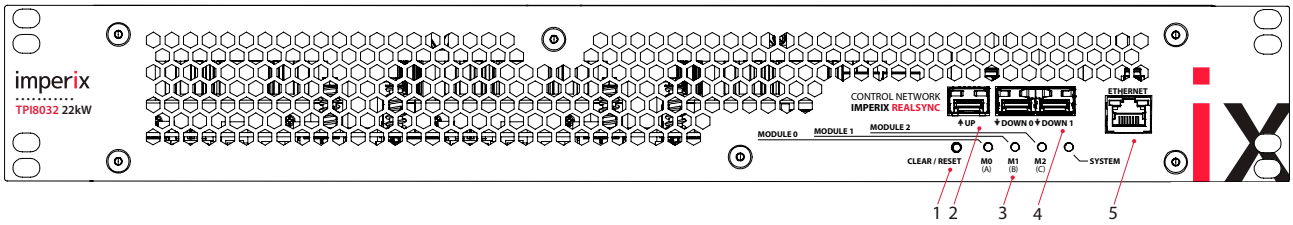

Fig. 1. Front panel view of the TPI8032

1) Clear/reset push button
2) SFP interconnect – UP link
3) System and power modules status LEDs
4) SFP interconnect – DOWN links
5) Gigabit Ethernet port (RJ45)

BACK PANEL

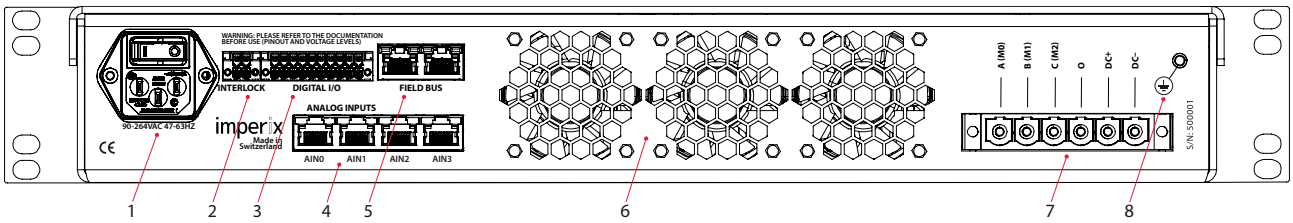

Fig. 2. Back panel view of the TPI8032.

1) AC mains switch and socket (IEC C14, 90-264V, 47-63 Hz)
2) Electrical interlock connector (IN/OUT)
3) GPI/GPO port
4) Analog inputs (RJ45, ±5V)
5) Field bus ports (RJ45)
6) Fan outlets
7) DC/AC power connector
8) Earth (ground) terminal

DEVICE CONTENT

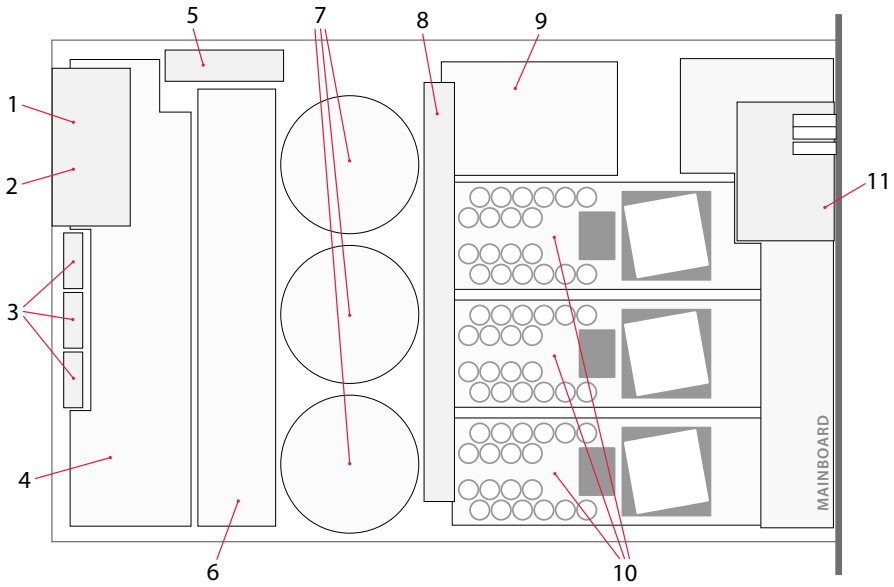

Fig. 3. Simplified system description of the TPI8032.

1) Digital I/Os (top PCB)
2) Analog inputs (bottom PCB)
3) Rear fans
4) Precharge circuit and AC measurements
5) Auxiliary supply
6) AC EMC filter
7) Main inductors
8) Bus bars
9) DC EMC filter
10) Power modules (half-bridges)
11) B-Board PRO embedded controller

FUNCTIONAL OVERVIEW

CONTROL STAGE

The embedded B-Board PRO controller is the main processing unit. It is responsible for loading and executing the application code developed by the user. Additionally, the mainboard interconnects the B-Board to the rest of the system and carries the following groups of signals:

- Control signals include analog measurements, gating signals, and relay commands exchanged by the main controller and the power stage.
- Fault signals are aggregated by the coordination unit micro-controller and shared across the system.
- I/O signals correspond to the digital and analog connectivity provided at the rear of the enclosure.

POWER STAGE

The power stage consists of the following elements:

- Power modules : The inverter consists of three half-bridge modules with their DC bus capacitors.
- Main inductors : One per phase. They form an LC filter with the capacitors of the AC EMC filter.
- EMC filters : Reduce the electromagnetic interferences generated by the power modules.
- AC precharge circuit : Prevents the flow of uncontrolled rectified currents through the anti-parallel diodes of the MOSFETs.
- Sensors : Ten voltage and current sensors are distributed along the converter, as shown in Fig. 4.

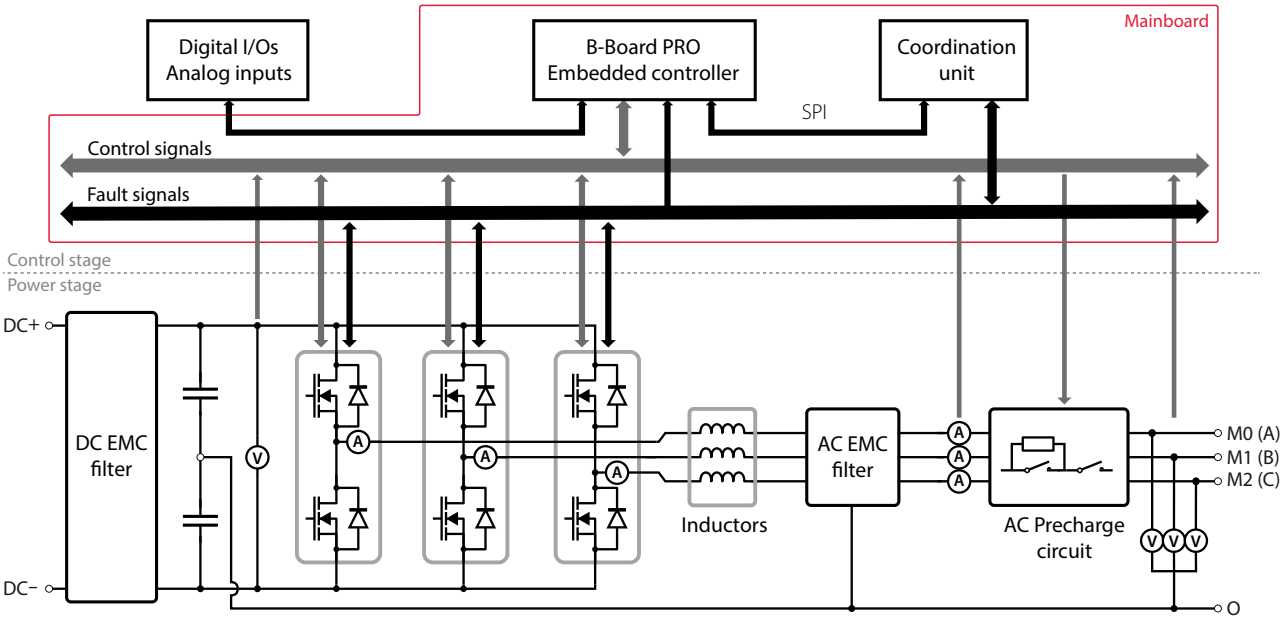

Fig. 4. Functional overview of the TPI8032.

MAIN COMPONENTS

Component	Devices	Main specifications
Main processing unit	*1x B-Board PRO*	*Xilinx Zynq processor – See below or device datasheet*
Power switches	*6x On Semiconductor NTHL020N120SC1*	*SiC MOSFET – See below or device datasheet*
DC bus capacitors	*3x 500uF @800V (3x 2 banks of 10x100uF)*	
Drivers	*6x Texas Instruments ISO5452-Q1 (per phase)*	*2.5 A, 100 kV/µs, VIORM = 1.42 kVPEAK, VIOTM = 8 kVPEAK*
DC bus voltage sensor	*1x Resistive divider + Avago ACPL-C87B*	
Power module current sensors	*3x ACEINNA MCA1101-50-3*	
AC current sensors	*3x Shunt + AMC3306M05*	
AC voltage sensors	*3x Resistive divider + AMC3336*	
Main inductors	*3x HKR VD01400-B, 950 µH*	
Precharge resistors	*3x 51R, ±5%, 20W*	
Damping resistors	*3x 10R, ±5%, 20W*	
AC and DC fuses	*3x 32 A (AC side), 2x 32 A (DC side)*	*6.3 x 32 mm fuses, slow blow*

Table 1. Main components of the TPI8032.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Test conditions	Max.	Unit
Maximum DC bus voltage	$V_{DC,max}$	Power modules not switching	900	V
Maximum transient DC isolation voltage (1 min)	$V_{DC,transient}$		1.65	$kV_{LL,PEAK}$
AC line-to-line clamping voltage	$V_{LL,max}$	8/20µs impulse current (1mA)	1.0	$kV_{LL,PEAK}$
Maximum residual current [1]	$I_{rc,max}$		30	mA
Highest allowable junction temperature	$T_{J,max}$		175	°C
Maximum permissible operating temperature of common mode inductors	$T_{cm,max}$		125	°C
Continuous total power dissipation per leg	$P_{cooler,max}$		140	W
Precharge and damping resistors short time overload	$P_{resistor,max}$	Per phase, 10x rated power for 5 sec.	200	W

Table 2. Absolute maximum ratings of the converter.

CONVERTER SPECIFICATIONS

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
DC bus voltage [2]	V_{DC}		0	800	850	V
AC line-to-line voltage	V_{LL}	$V_{DC} = 800$ V		400	560	V_{RMS}
AC fundamental frequency	f_N			50		Hz
Switching frequency	f_{SW}	$V_{DC} = 800$ V	50		150	kHz
		$V_{DC} < 800$ V Derating curves apply (page 8)	10		200	kHz
Maximum continuous phase current [3]	$I_{leg,max}$	$T_C = 100$ °C, $f_{SW} = 50$ kHz Reverse conduction in the channel [5]		32		A_{RMS}
Maximum DC bus ripple current [4]	I_{RIPPLE}	$f = 120$ Hz		8.0		A_{RMS}
		$f = 100$ kHz		16.0		A_{RMS}
Maximum continuous power	$P_{inverter,max}$	V_{LL}=400 V, $f = 50$ Hz, $I_{leg} = 32$ A 1h at room temperature starting at $T_a = 25$°C [6]		22		kW

Table 3. Converter specifications

CONTROLLER MAIN SPECIFICATIONS

Component	Specification
System on chip	Xilinx Zynq XC7Z030-3FBG676E
Processing system	ARM Cortex A9 1 GHz x2 1GB DDR3
Programmable logic (FPGA)	Kintex 7 125K (user programmable)
Storage	Flash 16MB x2 micro SD + eMMC 8GB
Communication	Ethernet 1Gbps x1 SFP+ 5 Gbps x3
Fault inputs / outputs	Electrical interlock (3.3V) x1

Component	Specification
PWM outputs	Electrical (3V3) x32 Various modulators 4 ns resolution
Analog inputs	16 bits, simultaneous sampling x8 2 Msps (maximum speed) / 500 ksps (B-Box compatibility mode)
General-purpose digital outputs (GPO)	Electrical (5.0V) x8
General-purpose digital inputs (GPI)	Electrical (5.0V) x8

Table 4. Main system specifications for the B-Board embedded controller.

[1] The TPI8032 must be protected by an external differential circuit breaker. Additionally, the maximum residual current accepted by the circuit breaker must be chosen according to local regulations.
[2] The maximum DC bus voltage is defined by the specifications of the bus capacitors. Therefore, as for any aluminum electrolytic capacitors, few short-term over-voltages can be tolerated, provided that they involve limited amounts of energy.
[3] In cold conditions, the maximum current is limited by the power semiconductors. Otherwise, the current rating of the inverter is limited by the power envelope of the cooling solution.
[4] The maximum ripple current is defined by the equivalent series resistance (ESR) of the capacitors and relates to Joule losses and lifetime considerations. Therefore, this value can be temporarily exceeded, provided that the operating temperature of the capacitors remains low.
[5] This indicates that both switches are actively used and that reverse conduction inside the MOSFET channel is used in order to reduce the conduction losses.
[6] The specification is valid when the converter is used for one hour at room temperature and placed on a table. When stacking multiple units or installing them in a cabinet, special cake must be taken to ensure sufficient airflow around the enclosure. The actual runtime strongly depends on environmental conditions.

FILTERING SOLUTION

Power modules generate electromagnetic emissions (conducted and radiated) that interfere with other nearby equipment. It typically leads to distorted analog measurements and bit flips in digital signals. These emissions are mostly due to the PWM operation of the semiconductors and the related common-mode currents. To mitigate these effects, the TPI is equipped with two EMC filters on the AC and DC sides (see Fig. 5).

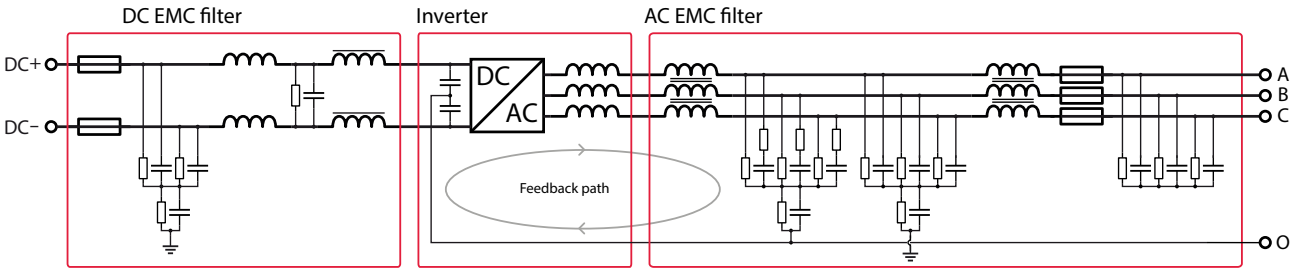

Fig. 5. Schematic overview of the filtering solution.

DC EMC FILTER

The main role of the DC filter is to limit the transmission of the input common-mode current from the DC side to the AC output (and vice-versa). This goal is achieved by providing a low-impedance path to the ground at the filter's input. Additionally, the DC filter has a CLC structure in differential mode to filter out the HF noise. The structure of the filter is shown in Fig. 6.

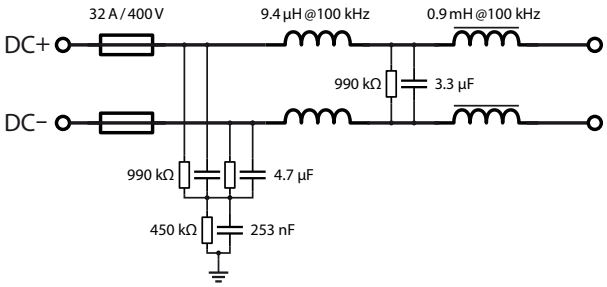

Fig. 6. Structure of the DC EMC filter.

AC EMC FILTER

Similarly, the AC filter limits the *input* common-mode current coming from the AC side with an LC stage. However, it's main role is to limit the *output* common-mode current from the converter by providing a low-impedance path through the feedback path. The structure of the filter is shown in Fig. 7.

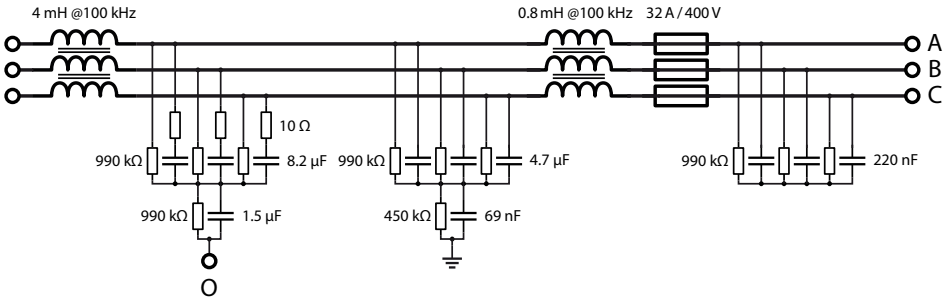

Fig. 7. Structure of the AC EMC filter.

MAIN INDUCTORS

Besides electromagnetic compatibility considerations, there is a need to filter the AC output in differential mode to limit the harmonic content. To this end, three 950 µH main inductors were placed between the power modules and the AC filter to form an LC filter.

WARNING:
The AC EMC filter is meant for three-phase, three-wire operation. Connecting the neutral point of the AC load to the DC bus midpoint O is possible but may lead to the saturation of the common-mode inductors, thereby reducing the effectivness of the filter.

CISPR 11 EMC COMPLIANCE

The TPI complies with the CISPR 11 international standard for electromagnetic emissions from Industrial, Scientific, and Medical (ISM) equipment.
According to this standard, the TPI is a Group 1 Class A piece of equipment. As such, it is suitable for use outside residential environments and does not generate RF energy on purpose.

The conducted emission limits for 20-75 kVA devices from Group 1 Class A are shown in Fig. 8. They are expressed in [dB (µV)] and cover frequencies from 150 kHz to 30 MHz. Furthermore, the average (AVG) and quasi-peak (QP) noise is measured in accordance with CISPR 16-1. Fig. 8 shows the result of the EMC qualification test for the TPI.

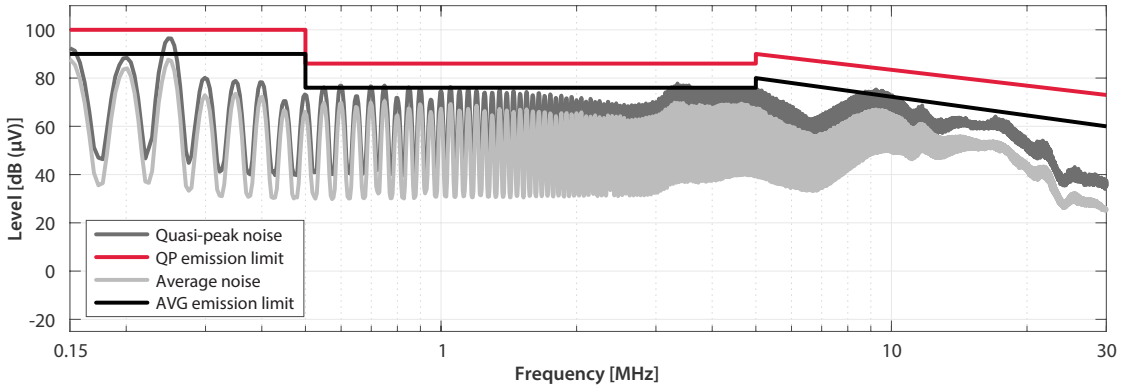

Fig. 8. Conducted emissions of the TPI in compliance with CISPR 11.

POWER SEMICONDUCTORS SPECIFICATIONS

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
MOSFET drain-source on-state resistance	$R_{DS(on)}$	I_{DS} = 32 A, T_J = 25°C		21	25	mΩ
		I_{DS} = 32 A, T_J = 150°C		29	40	mΩ
Diode forward voltage	V_F	I_{SD} = 32 A, T_J = 150°C		3.5		V
Peak reverse recovery current	I_{RRM}	I_{SD} = 32 A, V_R = 800 V, V_{GS} = -5 V		24		A
Reverse recovery delay	t_{RR}			31		ns
Turn-on losses	E_{on}	I_D = 32 A, V_{DS} = 800 V, $R_{g(ext)}$ = 10 Ω		370		µJ
Turn-off losses	E_{off}	V_{GS} = -5/20 V		390		µJ
External gate resistance	$R_{g,on}$			10		Ω
	$R_{g,off}$			5		Ω

Table 5. Main specification of the power semiconductors.

AC PRECHARGE CIRCUIT

The inverter naturally acts as a diode rectifier due to the anti-parallel body diodes of the MOSFETs. Uncontrollable currents will flow through the diodes should the DC bus voltage drop below the rectified AC voltage. For this reason, it is essential to precharge the DC bus before initiating regular operation.
The AC precharge circuit consists of a three-phase set of resistors in series with the AC input (see Fig. 9). They limit the input current during the precharge and are later bypassed to avoid unnecessary losses during regular operation.
By default, the RLY driver automates the precharge procedure and automatically disconnects the converter when the DC bus voltage drops below the rectified voltage (see page 18). Alternatively, it is possible to have direct control over the precharge and bypass relays.

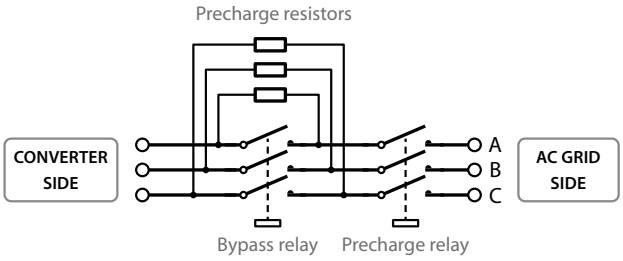

Fig. 9. Schematic of the AC precharge circuit.

Characteristic	Min.	Typ.	Max.	Unit
Precharge resistors		51		Ω
Relays closing time, incl bounce time			18	ms
Relay opening time, incl bounce time			15	ms
Precharge time		1.2	4	s

Table 6. AC precharge circuit specifications.

EMBEDDED SENSORS

DC BUS VOLTAGE MEASUREMENT CIRCUIT

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Nominal measured voltage	*On-board isolation*	*0.0*		*850*	*V*
Measuring range		*0.0*		*980*	*V*
Nominal sensitivity			*4.99*		*mV/V*
Sensitivity error	*Including resistive divider*		*±2.0*		*%*
Signal bandwidth	*-3 dB*		*10*		*kHz*
Measurable slope			*170*		*V/µs*

Table 7. Main specifications of the DC bus voltage measurement circuit.

POWER MODULES CURRENTS MEASUREMENT CIRCUIT

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Nominal measured voltage	*On-board isolation*		*±32.0*		A_{RMS}
Measuring range			*±60.0*		A_{RMS}
Nominal sensitivity			*50*		*mV/A*
Sensitivity error			*±0.4*		*%*
Signal bandwidth	*-3 dB*		*360*		*kHz*
Measurable slope			*133*		*A/µs*

Table 8. Main specifications of the power modules currents measurement circuit.

AC CURRENTS MEASUREMENT CIRCUIT

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Nominal measured voltage	*On-board isolation*		*±32.0*		A_{RMS}
Measuring range			*±50.0*		A_{RMS}
Nominal sensitivity			*39.06*		*mV/A*
Sensitivity error	*Including shunt*		*±1.2*		*%*
Signal bandwidth	*-3 dB*		*200*		*kHz*
Measurable slope			*103*		*A/µs*

Table 9. Main specifications of the AC currents measurement circuit.

AC VOLTAGES MEASUREMENT CIRCUIT

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Nominal measured phase voltage	*On-board isolation*		*±230*		V_{RMS}
Measuring range			*±390*		V_{RMS}
Nominal sensitivity			*2.54*		*mV/V*
Sensitivity error	*Including shunt*		*±0.8*		*%*
Signal bandwidth	*-3 dB*		*200*		*kHz*
Measurable slope			*158*		*V/µs*

Table 10. Main specifications of the AC voltages measurement circuit.

SAFE OPERATING AREA

The operating conditions are constrained by the converter Safe Operating Area (SOA). The limitations on the DC bus voltage, AC output voltage, and switching frequency are illustrated in Fig. 10 to 13.

CURRENT DERATING

The maximum continuous current depends mostly on the cooling capability of the power semiconductors. When switching losses increase, conduction losses must be reduced according to Fig. 10 and 11 to ensure proper cooling. Additionally, further derating due to the ambient air temperature or other environmental conditions may apply.

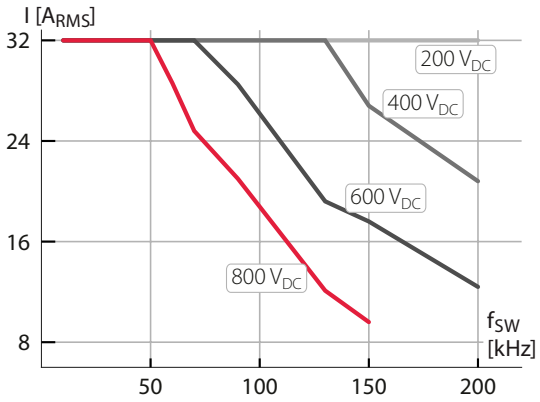

Fig. 10. Current capability as a function of the switching frequency

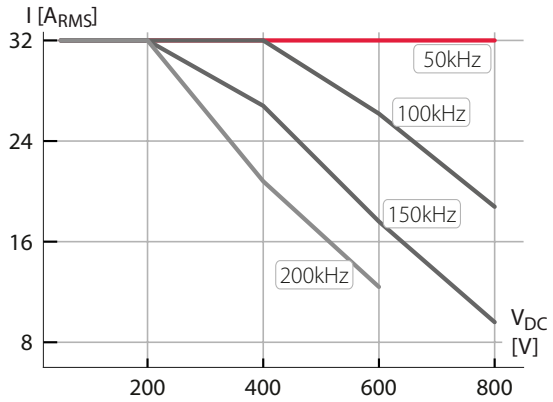

Fig. 11. Current capability as a function of the DC-bus voltage

DC BUS VOLTAGE DERATING

The EMC filters are designed to operate at 50 kHz or above. However, it is possible to operate the converter at a lower switching frequency by reducing the DC bus voltage (see Fig. 12). Operating the filters above the derating curve will saturate the common mode inductors and might overheat them.

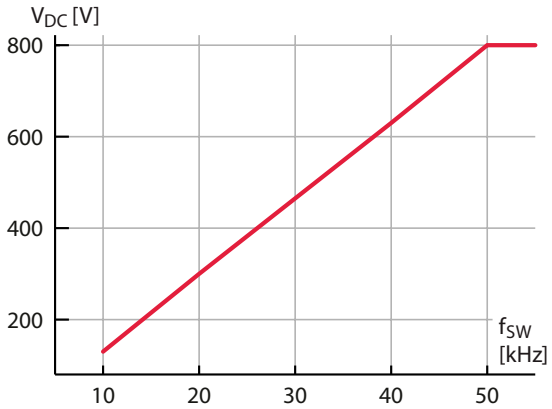

Fig. 12. DC bus voltage derating under 50 kHz.

AC OUTPUT VOLTAGE DERATING

The current flowing through the capacitors AC filter depends on the voltage amplitude and AC fundamental frequency. The higher the frequency, the lower the impedance of the capacitors. As a result, the power dissipation in the 10Ω damping resistors can exceed their 20W rating. Fig. 13 indicates the maximum AC voltage that can be applied at a given frequency to respect the rating of the damping resistors.

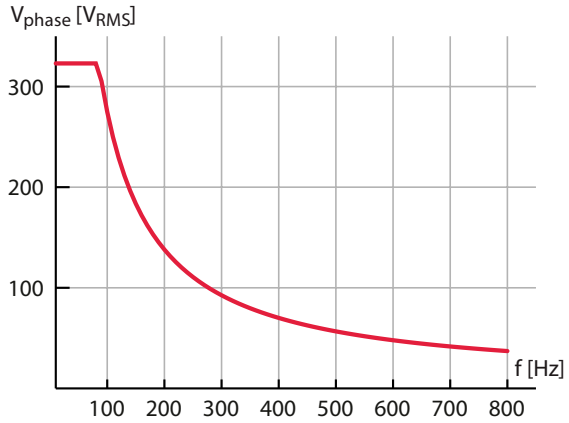

Fig. 13. AC output phase voltage derating as a function of the fundamental frequency.

WARNING:

Fig. 13 assumes that a single frequency is applied. When combining multiple harmonics, the total power dissipation must be considered. For this reason, the TPI implements an overcurrent protection for the damping resistors (see Tab. 13).

EMBEDDED LOGIC AND PROTECTION

PROTECTION LAYERS

Protection mechanisms are distributed across the system (see Fig. 14) and can be separated into three different layers:

- **Power modules** : Each inverter leg implements local over-current, over-voltage, and over-temperature detections to protect the semiconductors and the DC bus. These protections act as last resort protection.
- **Coordination unit** : A microcontroller (MCU) on the main board aggregates fault signals from the power modules and shares the fault across the entire system. Also, this MCU manages the status LEDs and the cooling of the enclosure.
- **B-Board controller** : The main processing unit enforces the SOA curves from Figures 10 and 12. Additionally, it provides an over-current protection for the damping resistors and automates the operation of the AC precharge.

POWER MODULE LOGIC

The digital supervisory system of each module implements the following functionalities:

- **Local fault detection** is managed by an MCU that continously monitors the current and voltage. Upon detection of an overvalue, the associated flag is raised to notify the coordination unit.
- **Fan/temperature management** is performed by a second MCU that monitors the cooler's temperature and adjusts the fan speed accordingly.
- **Gating signals generation** is handled by a CPLD. It evaluates the validity of the PWM signals ('H=1' and 'L=1' at the same time is forbidden) and generates the final gating signals. In case of a fault, the CPLD enforces a blocked state and raises the corresponding fault flag to notify the coordination unit.

FAULT SIGNAL SHARING AND CLEARING

The coordination unit is responsible for gathering the fault flags raised by the power modules. The full list is given in Tab. 11.

Event	Fault triggering when
Over-voltage	$V_{DC} > 850\,V$
Over-current	$\lvert I_M \rvert > 55\,A$
Desaturation	$V_{DS} > 2.8\,V$ *on either switch during 'on' state (corresp. to* $I_D > 80\,A$ *OR a shoot-through)*
Bad power supply	$V_{5V} < 4.5\,V$ *or* $V_{5V} > 5.5\,V$
	$V_{12V} < 11\,V$ *or* $V_{12V} > 13\,V$
Over-temperature	$T > 80°C$
Fan error	*Tachometer feedback lost*

Table 11. Faults from the power modules.

In addition to the previous task, the coordination unit ensures the proper cooling of the enclosure using the rear fans and can generate its own fault flags (see Tab. 12).

Event	Fault triggering when
Over-temperature	$T > 120°C$
Temperature error	*Sensor not connected*
Rear fan error	*Tachometer feedback lost*
Interlock	*External fault propagated through the electrical interlocking system*

Table 12. Faults from the coordination unit.

All fault flags are combined into a single global fault signal that is shared between the power modules and the main processing unit.
When a fault is detected, it is automatically cleared after a power-cycle of the TPI or when the clear/reset button, located on the front panel, is pressed. If the fault is still present, the converter will stay in a fault state.

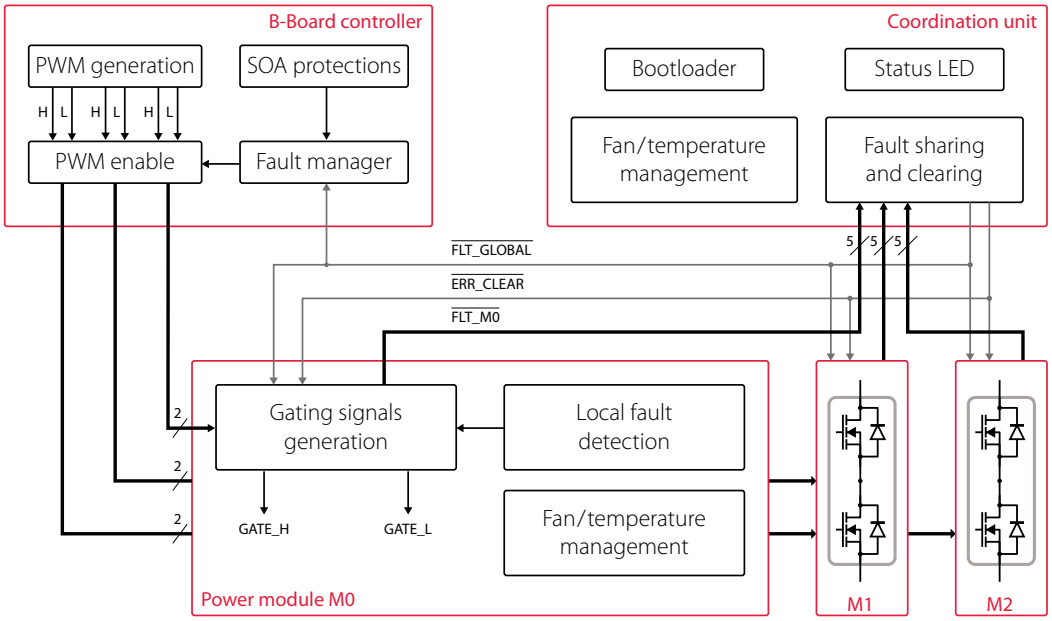

Fig. 14. Functional overview of the protection mechanisms.

SAFE OPERATING AREA PROTECTIONS

The B-Board continuously monitors the DC bus voltage and power modules currents and estimates the switching frequency from the gating signals. Therefore, it can detect if the inverter is operating outside the SOA curves from Fig. 10 and 12 and generate a fault.
Additionally, the controller estimates the differential and common mode current flowing through the damping resistors to implement over-current protection.
The SOA protections are implemented in FPGA and listed in Tab. 13. Since they do not depend on the coordination unit, the SOA faults are directly reported in Cockpit (imperix's monitoring software).

Event	Fault triggering when
Current derating curve exceeded	$\|I_M\| > \|I_{M,max}(V_{DC}, f_{sw})\|$, *see Fig. 10*
DC bus derating curve exceeded	$\|V_{DC}\| > \|V_{DC,max}(f_{sw})\|$, *see Fig. 12*
Over-current damping resistors	$\|I_{DR,DM}\| > 4$ *A, differential current*
	$\|I_{DR,CM}\| > 1.4\ A_{RMS}$, *common-mode current*

Table 13. SOA faults from the B-Board controller.

STATUS LEDS

Four LEDs are present on the front panel of the enclosure to indicate the status of the converter (see Tab. 14):

- M0 (A), M1(B), and M2(C) indicate the status of each power module independently. However, they are also be used together to indicate an event that affects the entire converter.
- SYSTEM is directly controlled by BBOS, the real-time operating system. By default, it indicates the Core state when a code is running. However, it can also display the synchronization status when the TPI is part of a distributed control network.

ERRORS AND WARNINGS

Faults from the power stage are separated into two categories:

- Errors are critical faults that immediately blocks the gate driver signals.
- Warnings do not pose an immediate threat to the converter. Thus, a warning flag must be raised for at least one second before triggering a global fault. Faults caused by a warning are indicated in orange.

CORE STATE

The Core state from BBOS indicates the status of the converter:

- FAULT : The controller received an error signal. The user must clear the fault to switch back to the BLOCKED state.
- BLOCKED : PWM outputs are blocked. The converter is ready to operate and waits for the enable command to switch to the OPERATING state.
- OPERATING : PWM outputs are enabled.

SYNCHRONIZATION STATUS

Multiple imperix controllers can operate as part of a distributed control network using SFP communication links. Whenever the TPI detects that it is part of a network, it will enter a discovery phase to determine its position in the network topology and synchronize its clock with the other controllers. Each controller also receives a unique identifier called the device ID based on its position within the network.
The synchronization status is indicated as follow:

- SYNCHRONIZING : The SYSTEM LED blinks in orange during the synchonization procedure. The latter can fail if the network topolgy is invalid or some devices have incompatible firmwares.
- STAND-BY : Upon successful synchronization, the TPI8032 advertises its ID by making the SYSTEM LED blink X times in green, with X corresponding to the device ID. If the device ID is #0, the LED does not blink.

Color	Blinking	M0 (A) LED	M1(B) LED	M2 (C) LED	M0-2 LEDs together	SYSTEM LED
None	*None*					*No code running*
Red	*None*					*Core state FAULT*
	Slow (1Hz)	*Over-current*	*Over-current*	*Over-current*	*DC bus overvoltage*	
	Fast (5 Hz)	*Desaturation or 1-1*	*Desaturation or 1-1*	*Desaturation or 1-1*	*Interlock*	
Orange	*None*					*Core state BLOCKED*
	Slow (1Hz)	*Over-temperature or fan error (module)*	*Over-temperature or fan error (module)*	*Over-temperature or fan error (module)*	*Over-temperature or fan error (enclosure)*	
	Intermediate (4Hz)					*Synchronizing*
	Fast (5 Hz)	*Bad power supply*	*Bad power supply*	*Bad power supply*		
Green	*None*	*No fault*	*No fault*	*No fault*		*Core state OPERATING*
	Slow (1Hz)					*Device ID*

Table 14. Color codes of the status LEDs.

BOOTLOADER

The coordination unit MCU is preloaded with a bootloader that dynamically loads the application code during the boot sequence. This mechanism allows updating the firmware of the MCU from the B-Board controller. When the system boots, an orange LED chaser is displayed on the front-panel while the bootloader loads the application code. Once this process is complete, all three LEDs M0 to M2 turn green, and the converter is ready to operate.

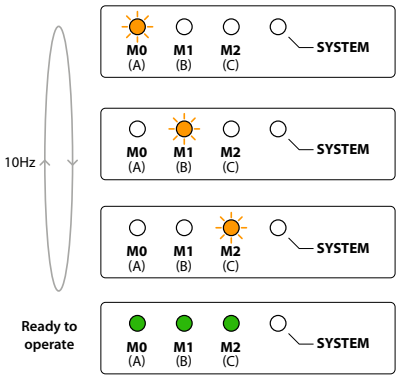

Fig. 15. Boot sequence status.

If a firmware update is available, the bootloader transfers it from the B-Board SD card to its persistent memory. This mechanism removes the need to send the application code after a power cycle and accelerates the startup process. The firmware update status is displayed on the front panel, as shown in Fig. 16.

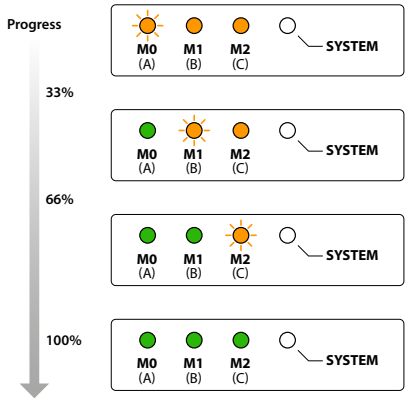

Fig. 16. Firmware update status.

B-BOARD LOGICAL STRUCTURE

The TPI operates thanks to an association between two CPU cores and dedicated peripherals implemented in programmable logic. The distribution of tasks is as follows:

- CPU0: Running on Linux, the first core is responsible for loading the application code, supervising the system execution and managing the data logging.
- CPU1: Running on BBOS (lightweight secured proprietary operating system), the second core executes the application-level control code developed by the user.
- FPGA: The programmable logic area contains all the application-specific peripherals. By default, the corresponding firmware is fixed.

The pre-implemented FPGA peripherals are as follows:

- CLK: Offers clock generators with up to four separate time-bases that can be used with other peripherals.
- ADC: Acquires data from the 10 internal voltage/current sensors and the 4 analog input channels.
- SBI: Provides easy-to-use access for inbound data traffic from the user-programmable area (sandbox).
- SBO: Provides easy-to-use access for outbound data traffic from the user-programmable area (sandbox).
- CB-PWM: Contains 3 user-configurable carrier-based modulators (conventional sampled PWM, complementary signals with deadtime).
- SB-PWM: Provides access to the PWM outputs from the user-programmable area (sandbox).
- GPO: Offers 8 General-Purpose Outputs.
- GPI: Offers 8 General-Purpose Inputs.
- RLY: Handles the AC precharge circuit.
- ETH: Supports data exchanges on Ethernet (TCP/UDP).
- CAN: Provides connectivity with CAN peripherals.

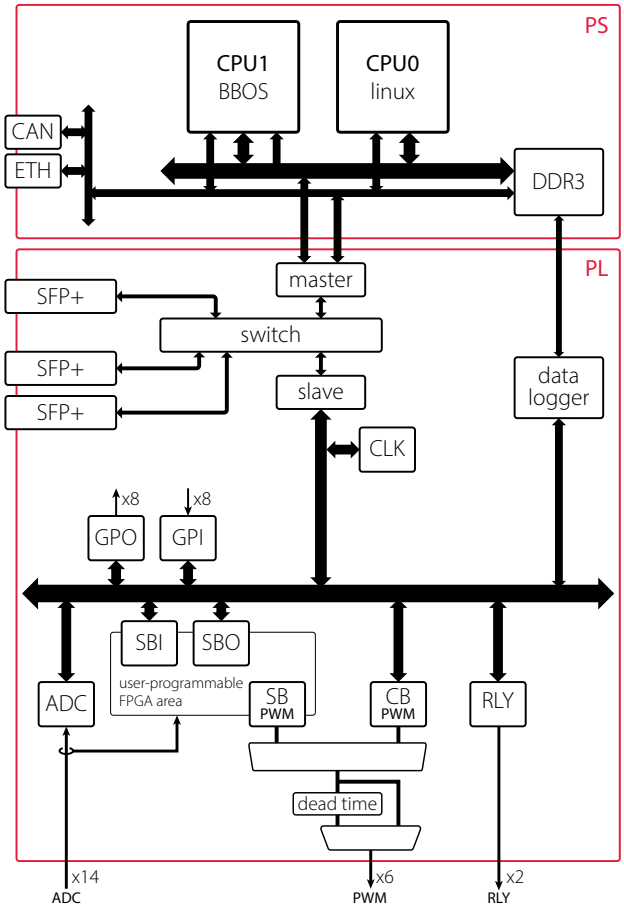

Fig. 17. Functional overview of the embedded B-Board controller.

CONTROL SIGNALS

Fig. 18 shows all the control signals exchanged between the main processing unit and the power stage.

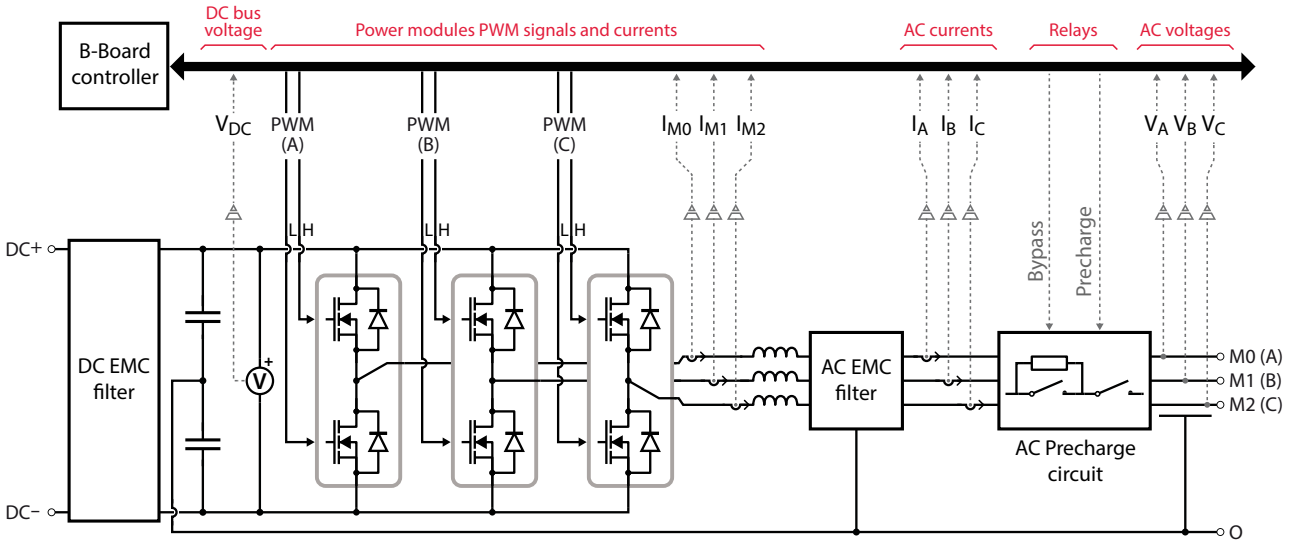

Fig. 18. Control signals exchanged by the control and power stages.

ANALOG CHANNELS

The TPI includes ten built-in analog measurements, as shown in Fig. 18 and supports up to 4 external sensors. It uses the two ADC chips embedded on its B-Board (2x 4 channels, SAR-type) and features 6 additional ADCs (ΔΣ-type). The analog channels assignment is given in Tab. 15.

Analog channel	ADC type	Symbol	Description
0	SAR	V_{DC}	DC bus voltage
1	SAR	I_{M0}	Power module current - M0 (A)
2	SAR	I_{M1}	Power module current - M1 (B)
3	SAR	I_{M2}	Power module current - M2 (C)
4	SAR	AIN0	External sensor #0
5	SAR	AIN1	External sensor #1
6	SAR	AIN2	External sensor #2
7	SAR	AIN3	External sensor #3
8	ΔΣ	V_A	AC voltage - Phase A
9	ΔΣ	I_A	AC current - Phase A
10	ΔΣ	V_B	AC voltage - Phase B
11	ΔΣ	I_B	AC current - Phase B
12	ΔΣ	V_C	AC voltage - Phase C
13	ΔΣ	I_C	AC current - Phase C

Table 15. Analog channels assignment.

ANALOG-TO-DIGITAL CONVERTER (SAR-TYPE)

The two successive-approximation (SAR) analog-to-digital converters of the B-Board are LTC2324-16 from Linear Technologies. The devices features 4 full-differential channels, each with a resolution of 16 bits, and guarantee simultaneous sampling on all channels. Overall performance specifications are given in Tab. 16. The retro-compatible mode exists to support B-Box RCP hardware prior to revision 3.5 (commercialized in 2020) when using multiple controllers in a networked configuration.

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Resolution			16		bits
Transient response	Full-scale step		30		ns
Conversion time	Retro-compatible mode		1.98		µs
	Full-performance mode		220		ns
Sampling rate	Retro-compatible mode	0.0		500	ksps
	Full-performance mode	1.0		2.0	Msps
Sampling jitter	Same B-Board		±2.1		ns
	Across all B-Boards		±3.6		ns
Data transfer delay		See Fig. 9.			ns

Table 16. Performance specifications of the A/D conversion.

ANALOG-TO-DIGITAL CONVERTER (ΔΣ-TYPE)

Two different models of delta-sigma (ΔΣ) analog-to-digital converters are in use: the AMC3306M05 for current sensing and the AMC3336 for voltage sensing, both from Texas Instruments. Unlike their SAR counterparts, ΔΣ modulators convert the analog input signal into a digital bitstream. Then, the bitstream is decimated with a sinc digital filter to obtain 16-bits data samples, which are re-synchronized with the SAR ADC samples. Overall performance specifications are given in Table 17.

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Input range	*AMC3306M05*		*±50*		*mV*
	AMC3336		*±1.0*		*V*
Modulator clock input (CLKIN)			*20*		*MHz*
Resolution	*Sinc digital filter*		*16*		*bits*
Data transfer delay		*See Fig. 9.*			*ns*

Table 17. Performance specifications of the A/D conversion.

EXTERNAL MEASUREMENTS

The analog chain of the external measurements is presented in Fig. 19. Additionally, the overall performances are indicated in Tab. 18.

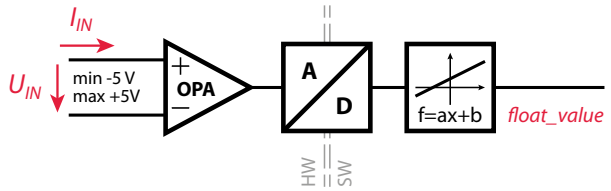

Fig. 19. Block diagram of external analog channels.

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Input voltage range	*Differential mode*		*±5.0*		*V*
	Common mode			*±12.5*	*V*
Max. tolerable voltage	*On any pin*			*±7.0*	*V*
Input impedance			*5.0*		*kΩ*
Signal bandwidth	*-3 dB*		*1.5*		*MHz*
CMRR	*<100 kHz*		*>80*		*dB*
	>100 kHz		*>65*		*dB*
Embedded power supply voltage		*±14.6*	*±15*	*±15.4*	*V*
Embedded power supply output current	*per channel*			*200*	*mA*
	all channels			*400*	*mA*

Table 18. Performance specifications of the analog inputs.

ANALOG INPUT CONNECTORS

Analog inputs rely on RJ45 connectors. This allows the use of well shielded twisted pair cables for the connection to sensors, with good EMC performance.

Pin	Pair	Color	Description
1	*2*	*orange stripe*	*+15 V*
2	*2*	*orange solid*	*+15 V*
3	*3*	*green stripe*	*0 V*
4	*1*	*blue solid*	*Positive input / current input*
5	*1*	*blue stripe*	*Negative input / ground*
6	*3*	*green solid*	*0 V*
7	*4*	*brown stripe*	*- 15 V*
8	*4*	*brown solid*	*- 15 V*

Table 19. Pinout of the analog inputs.

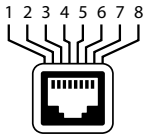

Fig. 20. RJ45 connector for analog inputs.

DATA TRANSFER PERFORMANCE

Data retrieval from A/D converters to the processing cores is achieved through FPGA logic and over the RealSync network in case of multi-device operation. Transfer delays vary with the amount of data to be transferred (see Fig. 2121). The overall delay from sampling to cache memory is therefore the sum of the ADC conversion time and data transfer delay.

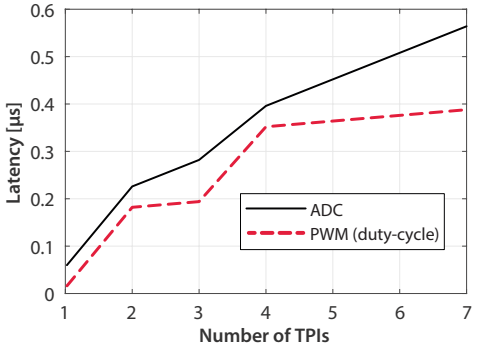

Fig. 21. Data transfert delay as a function of the number of TPI.

CLOCK AND INTERRUPT GENERATORS

Four independent clock generators are available on the TPI. They allow to configure independent time bases that can be allocated to various FPGA peripherals. This guarantees a very strict management of frequencies and phase-shifts between blocks. Clock generators support glitch-less re-configuration during run-time (variable-frequency).

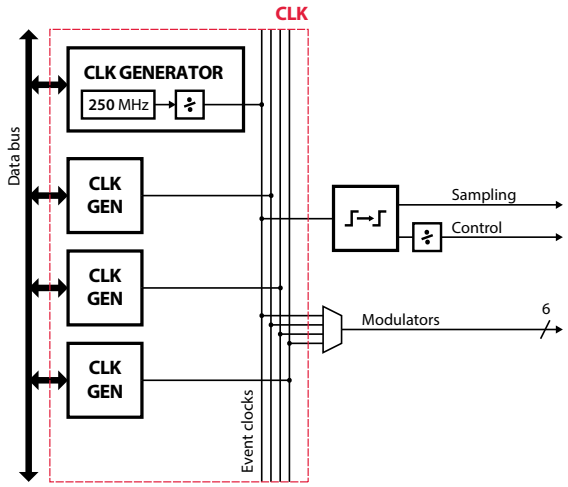

Fig. 22. Internal structure of the CLK peripheral block.

Outputs of clock generators are either interrupt signals or reference clocks for pulse-width modulators. Typical configurations include:

» **Basic example**: Control, modulation and sampling are at the same frequency. All resources are mapped onto the same clock generator. Measurements are made in the middle of the current ripple.

» **Multi-frequency example**: Two distinct converters are switching at different frequencies (e.g. 50 kHz and 60 kHz). Sampling is done at a common multiple (e.g. 300 kHz).

» **Variable-frequency**: One variable-frequency generator is used for modulation. Another frequency generator is used at a constant frequency for sampling and control.

Characteristic	Value
Counter resolution	*4.0 ns*
Counter depth (carrier, prescaler)	*16 bits*
Postscaler value (IRQ subsystem)	*0 – 4095*
Achievable frequency range	*58.2 mHz – 250 MHz*

Table 20. Performance specifications of the CLK peripheral block.

In a multi-device configuration (with stacked TPIs), all clock generators are intrinsically syntonized and automatically synchronized. This way, all phase-dependent operations such as sampling (ADC) or modulation (PWM) are guaranteed to have extremely accurate timings. Achievable performance is shown in Table 2121 and illustrated in Fig. 2323.

Characteristic	Min.	Typ.	Max.	Unit
Mean deviation, any slave TPI vs. master	*-2.0*	*0*	*2.0*	*ns*
Phase noise (jitter), any TPI, 3σ		*± 230*		*ps*

Table 21. Synchronization performance of CLK peripheral blocks across multiple TPIs using *RealSync*.

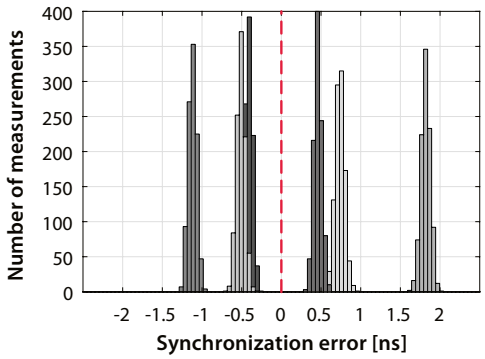

Fig. 23. Relative phase error performance with several TPIs in a stacked configuration (example with 6 slaves units).

WARNING:
By default, synchronous averaging is enabled on all ADC channels to improve noise rejection. However, this sampling method is only supported by CLK0. If any other clock is used, synchronous averaging is automatically disabled. More details can be found at *imperix.com/doc/help/synchronous-averaging*.

ELECTRICAL PWM CHANNELS

The converter has three PWM channels, which corresponds to six lanes (see Tab. 22). The modulators of the TPI generate pseudo-complementary signals for each phase.

PWM channel	PWM lane	Description
0	0	PWM High - Phase A (M0)
	1	PWM Low - Phase A (M0)
1	2	PWM High - Phase B (M1)
	3	PWM Low - Phase B (M1)
2	4	PWM High - Phase C (M2)
	5	PWM Low - Phase C (M2)

Table 22. PWM channels and lanes assignment.

By default, a fixed dead time is introduced between the '1' states of high and low gate drive signals. This mechanism ensures that two transistors of the same leg cannot be closed simultaneously.

Characteristic	Min.	Typ.	Max.	Unit
Dead time resolution		4		ns
Dead time value		124		ns

Table 23. Default specifications of the dead time generation.

Electrical PWM outputs are engineered to provide very high accuracy of timings. This is valid inside a PWM channel, across the whole bus, and even across all networked TPIs. Table 24 shows the performance specifications. Additional details regarding synchronization are given in the section addressing clock generation (page 14).

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Propagation delay asymmetry	Any two signals on same B-Board			±2.5	ns
	Any two signals across all networked B-Boards			±4.5	ns
Relative jitter	Any two signals on same B-Board			±0.4	ns
	Any two signals across all networked B-Boards			±0.7	ns

Table 24. Performance specifications of the PWM channels.

PULSE WIDTH MODULATORS

The B-Board controller embeds a full PWM signal generation system, featuring four sub-systems. Fig. 2424 depicts the corresponding structure:

- CB-PWM: Carrier-based modulators (3 channels with complementary signals). Various types of carriers are available, with single or double update rate. The CB-PWM block also provides hardware support for space-vector modulation (SV-PWM).
- SB-PWM: This subsystem connects with the user-programmable area (sandbox), which allows for the implementation of fully-customized modulation techniques. Easy-to-use I/O access from the software level is offered by the SBI and SBO blocks (see page 18).

At the output, each PWM signal goes through a dead time generator to avoid short-circuiting the inverter's legs. The only exception is the sandbox area, where the user can choose to implement their own dead time generator.

Dead time is obtained by delaying the rising edge of each PWM signal within a given pair. This results in an equivalent propagation delay of half the dead time.

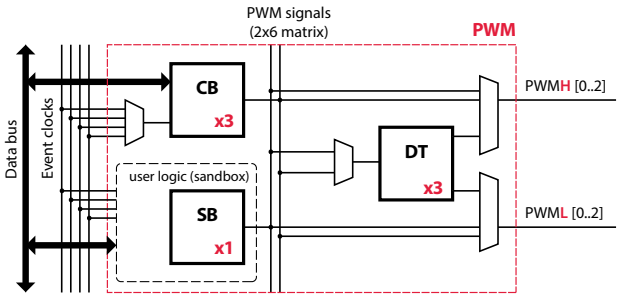

Fig. 24. Internal structure of the PWM signals generation block.

CB-PWM: CARRIER-BASED MODULATION

Carrier-based modulators offer the simplest way to generate pulse-width modulated signals. The corresponding subsystem features 3 independent modulators with complementary outputs. Each modulator offers independent duty-cycle and phase parameters as well as four different types of carriers. With triangular carriers, modulators can be configured with single or double update rates (once or twice per PWM period).

Characteristic	Value
Counter depth	16 bits
Edge resolution (counter resolution)	4 ns

Table 25. Performance specifications of the CB-PWM block.

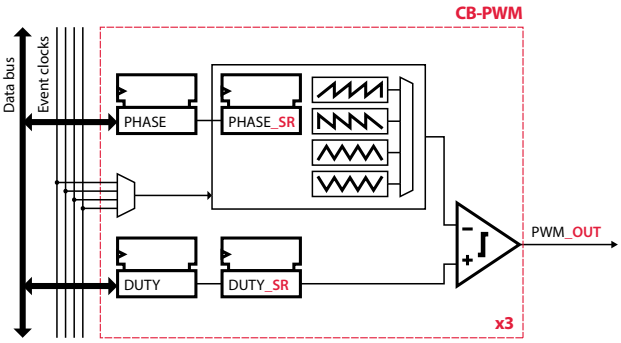

Fig. 25. Internal structure of the CB-PWM peripheral block.

SV-PWM: SPACE VECTOR MODULATION

Space vector modulation (sometimes referred to as SVM) is supported through dedicated software drivers, making use of the same resources as the CB-PWM subsystem. Indeed, once the closed vectors have been identified and the suitable sequence determined, the switching events can be easily produced by suitably-programmed modulators. SV-PWM automatically configures adjacent channels and supports single or double update rates.

SB-PWM : PWM ACCESS FROM THE SANDBOX

In addition to existing modulators, the B-Board also features a user-programmable area inside the FPGA . This notably allows to implement special own modulation techniques. In this sandbox, data read and write accesses from / to the CPU is provided from the SBI and SBO blocks, respectively (see "User-programmable area (Sandbox)" on page 18).
The SB-PWM subsystem itself allows to connect to the PWM lanes through the dead-time generator block (see Fig. 244) as well as the B-Board's hardware protection mechanisms.

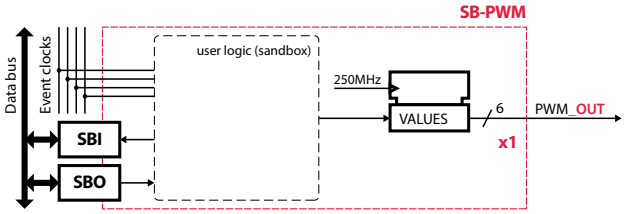

Fig. 26. Internal structure of the SB-PWM block.

DEAD TIME GENERATION SUBSYSTEM

As depicted by Fig. 2424, the PWM block features a dead time generator at its output. This subsystem can be either used or bypassed by picking-up the signals from the PWM signals matrix directly (SB-PWM only).
The dead time generation relies on a finite state machine operating as depicted in Fig. 2727. Essentially, rising edges of the high-side and low-side signals are delayed by a programmable amount of time. This results in an equivalent propagation delay of half the dead time.
Intrinsically, this implementation guarantees that a pulse shorter than the dead time value is not produced.

Characteristic	Min.	Typ.	Max.	Unit
Dead time resolution		*4*		*ns*
Dead time value	*0.004*		*262*	*µs*

Table 26. Performance specifications of the dead time generation.

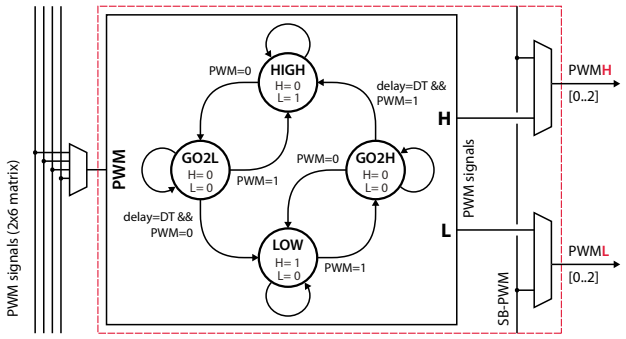

Fig. 27. Internal structure of the dead time generation block.

DATA TRANSFER PERFORMANCE

The transfer of continuously-updated modulation parameters from the processing core to the distributed modulators causes delays, which depend on the amount of data to be transferred. Fig. 2828 shows the achieved performance with respect to the update of the CB-PWM block. Other modulators perform similarly.

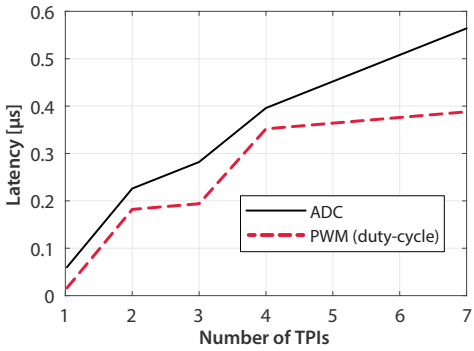

Fig. 28. Data transfer delay, as a function of the number of TPIs.

FAULT INTER-LOCKING SIGNALS

Fault inter-locking allows coordinating emergency mechanisms between a TPI and other appliances, or across several TPIs or systems. These mechanisms are bi-directional as they can inform other devices about an internal fault condition or reciprocally receive external trigger signals. Two types of inter-locking mechanisms are available on the TPI :

» Electrical inter-lock : Labeled **INTERLOCK** on the rear side of the device. The connector is part number 1787014 from Phoenix Contact. The mating part is 1790292.
» RealSync : In a stacked configuration with multiple networked TPIs, fault inter-locking between the controllers is natively available thanks to the imperix *RealSync* protocol (SFP optical fiber links).

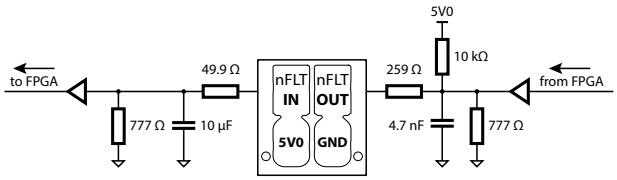

Fig. 29. Electrical circuit for the electrical inter-locking mechanism.

Characteristic	Medium	Min.	Typ.	Max.	Unit
Operating voltage	*Electrical*	*4.5*	*5.0*	*5.5*	*V*
Response delay to blocking of PWM signals	*Electrical*	*2.1*		*12.9*	*ms*
	RealSync		*0.25*		*µs*

Table 27. Performance specifications of the inter-locking.

DIGITAL INPUTS AND OUTPUTS

Electrical digital inputs and outputs are grouped on a single connector at the rear of the enclosure. Its part number is 1787098 from Phoenix Contact and the mating part is 1790373. The following functions are available:

» GPO: General purpose outputs (8 bits)
» GPI: General purpose inputs (8 bits)

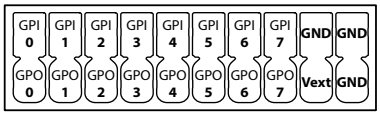

Fig. 30. Block diagram of the Controller Area Network peripheral.

GENERAL-PURPOSE OUTPUTS (GPO)

8 outputs are available and tied to the GPO block. The GPO signals are level shifted to 5V by default, but the logic level Vcc can be modified with an internal jumper (Fig. 31). It is possible to provide the supply voltage with an external source, using the pin Vext.

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Supply voltage Vcc		*4.5*	*5.0*	*35*	*V*
Output current, continuous	*Limited by package power dissipation*			*±1*	*A*
Speed			*45*		*Mbps*
Max. rise/fall time	*18V, 1000pF*			*16*	*ns*
Propagation delay asymmetry	*Any two signals on same B-Board*			*±2.5*	*ns*
	Any two signals across all networked B-Boards			*0.2*N*	*µs*

Table 28. Performance specifications of the GPO outputs.

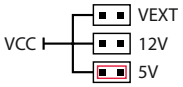

Fig. 31. GPO output voltage selection with an internal jumper.

WARNING:
Always pay attention to the **logic voltage level** of each signal. Refer to Tables 28 and 29 for detailed information. Unexpected behavior or damages may occur in case inappropriate voltage is applied to the TPI or any other circuit.

GENERAL-PURPOSE INPUTS (GPI)

8 inputs are available and tied to the GPI block. The logic level is clamped to 3.3V by a zener diode.

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Maximum tolerable input voltage				*26.7*	*V*
Speed			*45*		*Mbps*
Propagation delay asymmetry	*Any two signals on same B-Board*			*5.0*	*ns*
	Any two signals across all networked B-Boards			*7.0*	*µs*

Table 29. Performance specifications of the GPI inputs

CAN TRANSCEIVER

An isolated MCP2562FD-E/SN Controller Area Network (CAN) transceiver is available for communication between the TPI and third-party devices. Connectivity is provided through two RJ45 connectors on the rear side of the device for daisy-chained configurations.

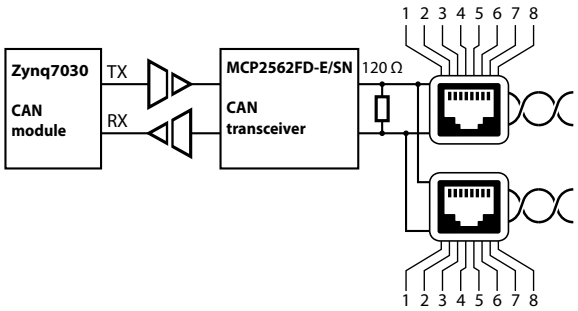

Fig. 32. Block diagram of the Controller Area Network peripheral.

Characteristic	Min.	Typ.	Max.	Unit
Operating baudrate			*8.0*	*MBd*
Tolerable voltage on CAN+ and CAN- pins	*-27.5*		*+27.5*	*V*
Bus impedance	*98.8*	*99.8*	*100.8*	*Ω*

Table 30. Performance specifications for the CAN transceiver.

Pin	Color	Description	Pin	Color	Description
1	*orange stripe*	*CAN H*	*5*	*blue stripe*	*NC*
2	*orange solid*	*CAN L*	*6*	*green solid*	*GND*
3	*green stripe*	*GND*	*7*	*brown stripe*	*NC*
4	*blue solid*	*NC*	*8*	*brown solid*	*NC*

Table 31. CAN pin/pair assignments.

RELAYS (RLY)

The DC bus voltage must be kept higher than the rectified AC voltage to prevent the flow of uncontrolled currents through the anti-parallel diodes of the MOSFETs. To this end, the operation of the AC precharge circuit is automated in the RLY driver and allows a safe connection to the grid. The Finite State Machine (FSM) is shown in Fig. 33.

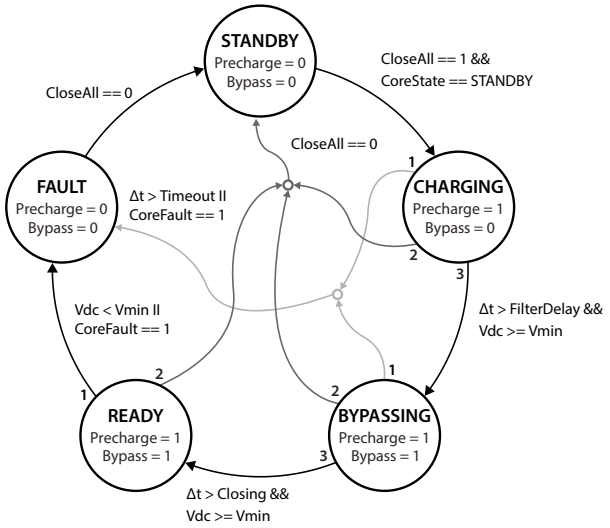

Fig. 33. Finite State Machine of the AC precharge circuit.

First of all, the AC rectified voltage is continuously estimated using the following equation:

$$V_{rectified}(t) = max(\,|V_A(t) - V_B(t)|\,,\,|V_B(t) - V_C(t)|\,,\,|V_C(t) - V_A(t)|\,)$$

From there, the minimum DC bus voltage required during operation is computed with the equation below. Essentially, the peak value of the rectified voltage is extracted and denoised with an averaging filter. Finally, a coefficient of 0.95 is applied to have some margin on the detection threshold.

$$V_{min} = 0.95 \times avg(\,max(\,V_{rectified}(\Delta t_{extract,peak})\,),\,\Delta t_{filter,delay}\,)$$

When the command to close the relays is received, the FSM executes the precharge procedure. Please note that it can fail due to external factors (e.g. a DC load that forces the DC bus voltage below V_{min}). This condition is detected with a timeout and sets the state machine into the FAULT state. If the precharge is successful, the state machine raises a *ready* flag to notify the CPU. This flag is made available to the user through the RLY driver. At this stage, it is safe to enable the PWM outputs. Table 35 summarizes the various delays.

Characteristic	Symbol	Value	Unit
Averaging filter delay	$\Delta t_{filter,delay}$	*1*	*s*
Peak voltage detection window	$\Delta t_{extract,peak}$	*20*	*ms*
Bypass relay closing time	$\Delta t_{closing}$	*200*	*ms*
Precharge timeout	$\Delta t_{timeout}$	*4*	*s*

Table 32. Precharge FSM delays.

Optionally, it is possible to control the precharge and bypass relays manually. By doing so, the user bears the risk of damaging the equipment in case of inadequate operation.

USER-PROGRAMMABLE AREA (SANDBOX)

The B-Board is designed such that its programmable logic area (PL) can embed user-defined logic. This may allow for the implementation of special modulation techniques, proprietary communication mechanisms, or interfacing with external hardware and components.

Within this special area, designated as *sandbox*, two peripheral blocks are pre-implemented for easy-to-use I/O access from / to the CPU cores:

- SBI: Input from the sandbox
- SBO: Output to the sandbox

Also, the sandbox offers connectivity to the following I/O:

- ADC values (8x 16 bits signed integers)
- SB-PWM signals (32 bits register)
- Internal clocks
- Physical I/Os (FLT, USR, GPI, GPO)

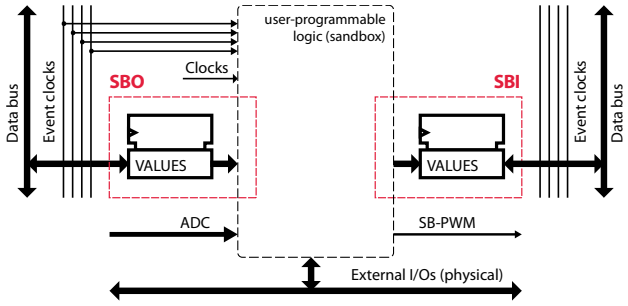

Fig. 34. Internal structure of the SBI and SBO blocks.

Thanks to the *RealSync* communication and synchronization protocol, the sandbox can be used indistinctively on the master or a slave B-Board within a control network. The data transfers (read or write) from the CPU core is handled by the SBI or SBO blocks using either the write-through (configuration) or write-back (real-time) data traffic, as with any other peripheral block.

C/C++ drivers (as well as their blockset counterparts) are readily available within the software development kits (SDKs). On the programmable logic side, development templates are provided upon request. In the provided HDL source code, other peripheral blocks are obfuscated.

WARNING:
The sandbox gives access to all FPGA resources of the B-Board, including some that are not available on the TPI (FLT, USR, SS-PWM, etc) or with a limited number of channels (ADC, PWM, GPI, and GPO).

INSTALLATION INSTRUCTIONS

HANDLING

The TPI is a heavy product and must be carried by two persons with proper caution. A risk of injury exists in case of fall on the lower limbs.

EARTHING

Careful earthing is essential for the proper operation of the EMC filters, as well as for personnel safety. The enclosure is electrically bonded to the protective earth conductor of the auxiliary power inlet. A ground (earth) terminal is also available on the rear panel and can be connected with a circular tab and an M4 screw.

CABLE CROSS-SECTION

Electric cables of sufficient section should always be used. Typically, a current density < 5A/mm^2 is recommended. For long connections or when a risk of fire is present, < 3A/mm^2 should be observed.

OVER-CURRENT PROTECTION

For some applications, such as when using this product for interfacing a power converter to the AC mains, fuse(s) or circuit breaker(s) must be present upstream, so that personnel safety is guaranteed at all times, and that risks or fire are mitigated.

PRODUCT SAFETY

FCC COMPLIANCE STATEMENT

This device is exempted from compliance with Part 15 of the FCC Rules, pursuant CFR47 §15.103(c) regarding industrial, commercial or medical test equipment.
CAUTION Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

CANADIAN COMPLIANCE STATEMENT

This digital apparatus is exempted from compliance with Canadian ICES-003, pursuant article 1.5.1(d). / Cet appareil numérique est exempté de conformité à la norme NMB-003 du Canada, ainsi que stipulé par l'article 1.5.1(d).

ENVIRONMENTAL CONDITIONS

The TPI is designed to be supplied with a 45W 90–264VAC power supply. Other environmental conditions are specified in Table 333.

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Input voltage		*90*		*264*	*V*
Power consumption		*5*		*45*	*W*
Inrush current				*0.7*	*A*
EMC performance	*CISPR11 Group 1 Class A*	*pass*			
Operating temperature		*0*		*35*	*°C*
Storage temperature		*0*		*50*	*°C*
Relative humidity	*Non-condensing*	*5*		*85*	*%*
Absolute humidity		*1*		*25*	*g/m³*
Overvoltage category	*OVC II*				
Mechanical protection	*IP20*				
Altitude				*2000*	*m*
Air pollution degree	*PD 2*				

Table 33. Environmental specifications for the TPI8032.

MECHANICAL DATA

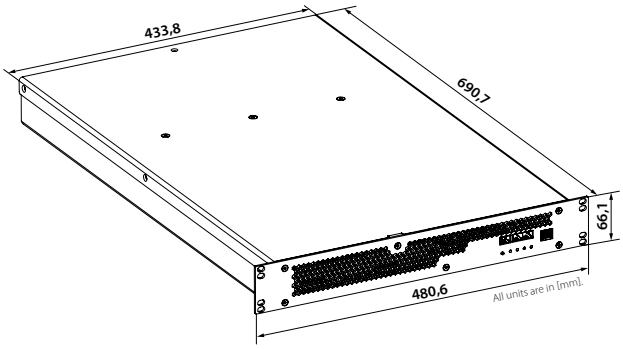

Fig. 35. Mechanical dimensions of the TPI8032.

Characteristic	Value	Unit
Weight	*23*	*kg*
Dimensions	*480.6 x 66.1 x 690.7*	*mm*

Table 34. Product dimensions.

INCLUDED ACCESSORIES

The TPI8032 22kW includes the following accessories:

» Ethernet cable (3m): To program and monitor the TPI from a PC.
» Single-phase power cord (2m): For auxiliary power. The plug type depends on the destination country.
» DC/AC power connector: The part number of the power connector is Phoenix Contact 1701977 and its mating part (delivered with the TPI) is 1913617. No cables are provided for the AC outputs and the DC bus.
» GPIO connector: The part number of the GPIO connector is 1787098 and its mating part (delivered with the TPI) is 1790373.
» Interlock connector: The part number of the interlock connector is 1787014 and its mating part (delivered with the TPI) is 1790292.

SOFTWARES

Programming the embedded controller requires either the ACG SDK (automated code generation from Simulink and PLECS), or the CPP SDK (C/C++). The corresponding licenses are sold separately.
The real-time monitoring software (imperix Cockpit) and the capability to edit the FPGA firmware are included in both SDKs, and do not require any additional license.



WARNING

This product must be used in electric / electronic equipment with respect to applicable standards and safety requirements in accordance with the manufacturer's operating instructions.



WARNING

Caution, risk of electrical shock! When using the devices, certain parts of the modules may carry hazardous voltages (e.g. power supplies, busbars, etc.). Disregarding this warning may lead to injury and / or cause serious damage.



WARNING

Risk of burns due to hot surfaces. Injury.

» Make sure the unit has cooled down before touching it.
» The device must be installed in an adequately ventilated space to ensure proper cooling.

REVISION HISTORY

» 31.08.23: Preliminary version
» 07.03.24: Updated specifications
» 19.11.25: Minor text changes

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ABOUT US

Imperix Ltd is a company established in Sion, Switzerland. Its name is derived form the Latin verb imperare, which stands for controlling and refers to the company's core business: the control of power electronic systems. Imperix commercializes hardware and software solutions related to the fast and secure implementation of pilot systems and plants in the field of power conversion, energy storage and smart grids.

NOTE

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