Dead time selection for imperix power modules

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This page presents a dead time selection method that can be used with imperix power modules. Appropriate dead time selection is crucial to guarantee the safety, reliability, and efficiency of a power converter.

Introduction

It is well known that the simultaneous conduction of two power semiconductors among the same phase-leg must always be avoided. Indeed, it would otherwise lead to extremely high currents due to this shoot-through condition, possibly damaging the semiconductors.

This critical situation is generally avoided by introducing a short non-conduction interval between the turn-off and turn-on events of both switches, here referred to as *dead time.*

The *dead time* must be sufficiently long to account for timing uncertainties (and variations) in the gate signal generation, as well as the switching behavior of the devices (e.g. with DC voltage, output current or temperature). However, the application of an excessive dead time generates non-negligible distortion on the output current as well as excessive losses.

Therefore, the proper selection of the *dead time* is an important task, which impacts directly the system efficiency as well as reliability.

This note provides step-by-step guidance to compute the minimal *dead time* value according to the control platform and power modules that are used.

Design objectives for dead time selection

The selection of the dead time is a delicate aspect of the control design, which must unavoidably be made as a trade-off between several aspects:

- An insufficient dead-time may lead to **shoot-through**, which is often linked to a high risk of damage for the semiconductors. This risk may be linked to normal or some very specific operating conditions.
- An excessive dead-time may induce excessive **distortion** on the voltage waveform (the amount of distortion if often proportional to the relative duration of the dead time versus the switching period).
- An excessive dead time may negatively impact the **system efficiency**, especially in applications where the diode conduction losses (during the dead time) are higher than the transistor conduction losses.

Facing the complexity of selecting the optimum dead time, this product note exclusively focuses on the safety-related aspect of shoot-through. As such, the chosen design guidelines are as follows:

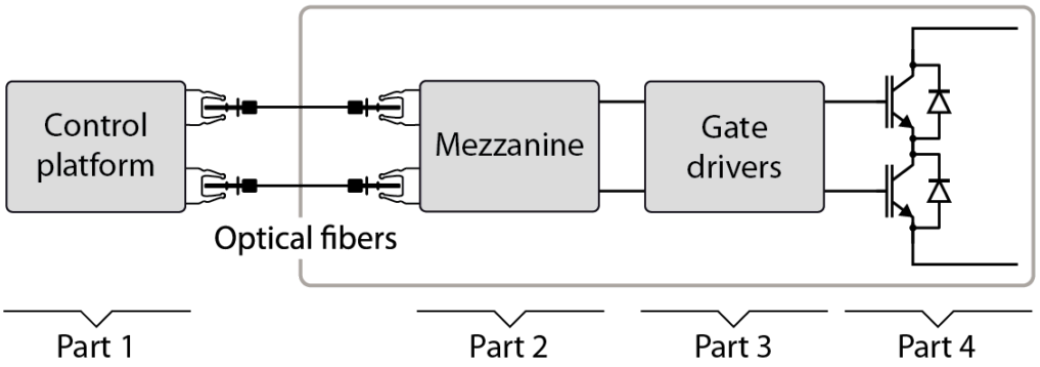
- The dead time is chosen to be a **constant parameter**, configured once at startup.
- The dead time is chosen **conservatively** to avoid any risk of shoot-through in a broad variety of applications. This approach may lead to a suboptimal choice in terms of distortion and efficiency.

The *going further* section of this note addresses possible improvements to the presented approach.

Design procedure

The proposed design procedure follows [1]. It sets the minimum possible dead time as a function of the turn-on/turn-off delay of the power semiconductors, as well as the asymmetry in the propagation delays of the gate signals across the whole chain from the digital controller to the gate drivers.

Referring to imperix products, the minimum possible dead time should be computed as the sum of four terms, corresponding each to a different part of the signal chain.



Elements along the PWM signal transmission chain

As proposed in [1], the minimal dead time can be computed using the following formula:

$$DT_{min} = (T_1 + T_2 + T_3 + T_4) \cdot 1.2$$

With the parameters:

- T_1 : the propagation delay asymmetry of the control platform (B-Box RCP or B-Board PRO);
- T_2 : the propagation delay asymmetry of the mezzanine board;
- T_3 : the propagation delay asymmetry of the gate driving state (related to the power module type);
- T_4 : the turn-on/turn-off times asymmetry of the IGBTs or MOSFETs;
- 1.2 : a safety margin equivalent to 20%.

Timing information

Part 1 – Control platform (PWM signal source)

For imperix digital controllers, the maximum propagation delay asymmetry is given in the device datasheets. The resulting information is summarized in the table below:

Control platform	T_1 [ns]
BoomBox 2 (optical PWM outputs)	36
B-Box RCP (hardware revision ≥ 3.0) on **optical** PWM outputs	13
B-Box RCP (hardware revision ≥ 3.0) on **electrical** PWM outputs	2.3
B-Board PRO (electrical PWM outputs)	t.b.d.

The propagation delay asymmetry between optical fibers **of the same length** is negligible. Indeed, the propagation speed of the PWM information (group delay) is about 5 ns per meter.

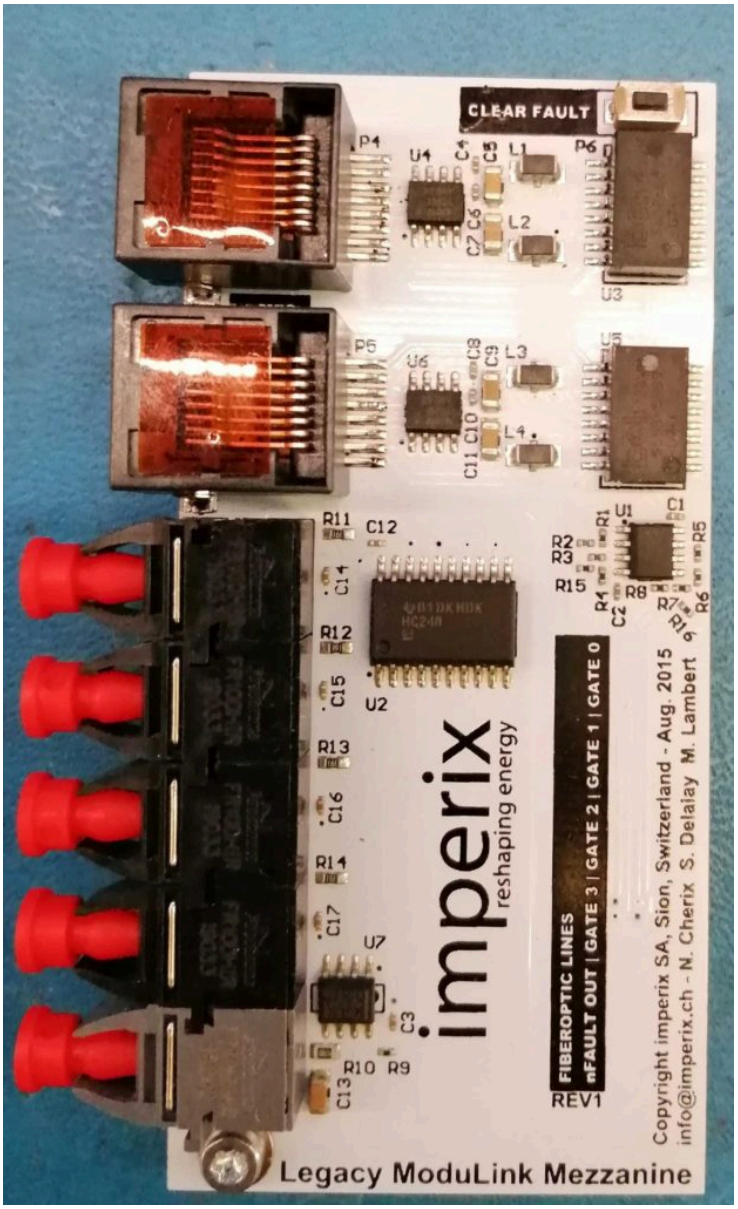
Part 2 – Mezzanine boards of imperix power modules (optical receivers)

The mezzanine boards are the small piggy-back modules that are present on the PEH- PEN- and newest PEB-based modules. The corresponding propagation delay asymmetry is given below:

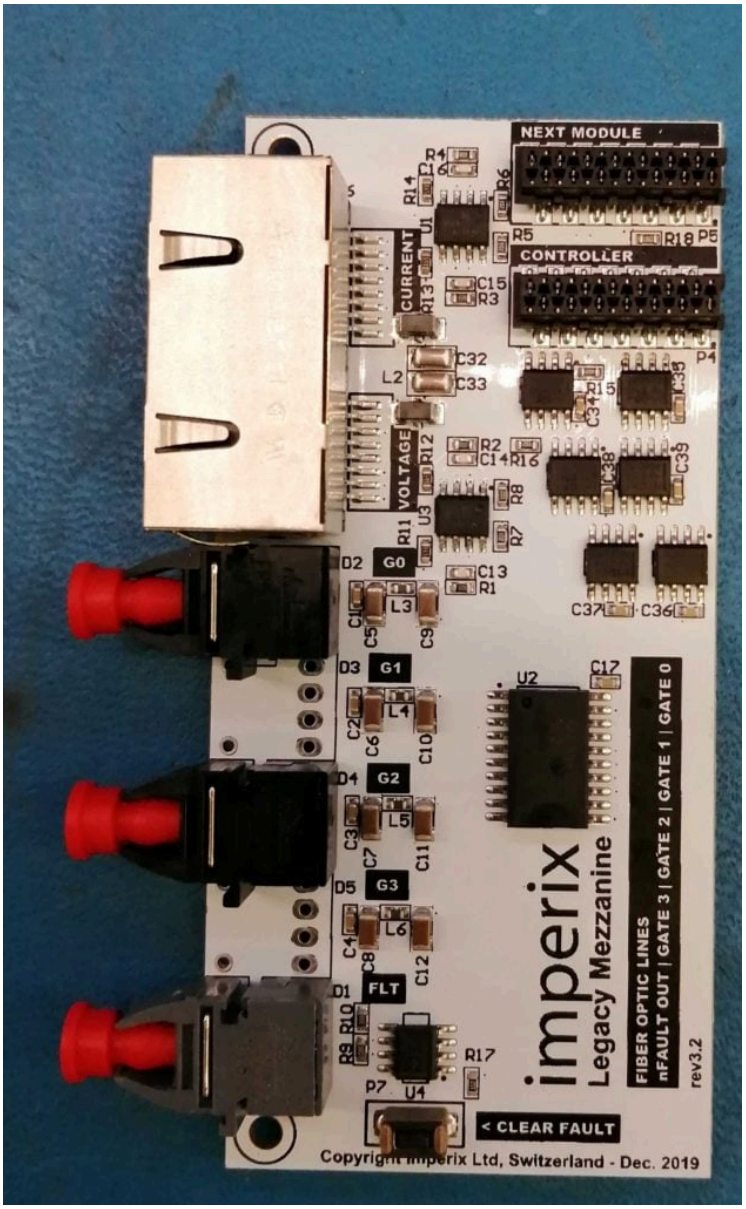
NB: The PEB 8032 and 4046 didn't require a mezzanine as the main board already hosts the optical receivers.

Mezzanine	T_2 [ns]
v.2	25
v.3	13
PEB 8032/4046 (legacy modules)	20

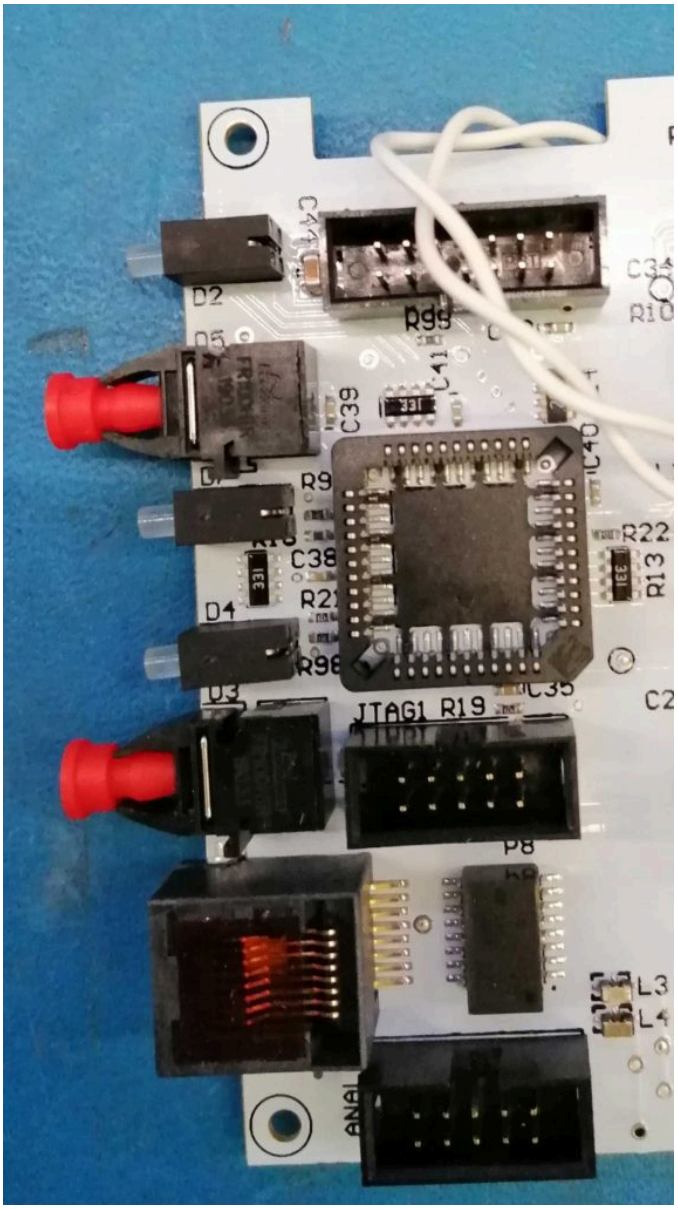
The pictures below show how to identify the mezzanine version:



Mezzanine v.2



Mezzanine v.3



No mezzanine

Part 3 – Power modules (CPLD and gate drivers)

For all modules, the gate signals are first processed by a CPLD before reaching the gate drivers. This CPLD is used for checking signal integrity and providing local protections. Subsequently, the PWM signals are processed by the gate drivers, resulting in an additional impact on the timings. The table below shows a summary of the overall propagation delay asymmetry as a function of the module type:

Power module	**T_3 [ns]**
PEB 8032 and 4046 (discontinued)	155
PEB 8024, 8038 and 4050	32
PEH 2015 and 4010	52

PEH 2015 – design **revision v.5** and older	502
PEN 8018	52

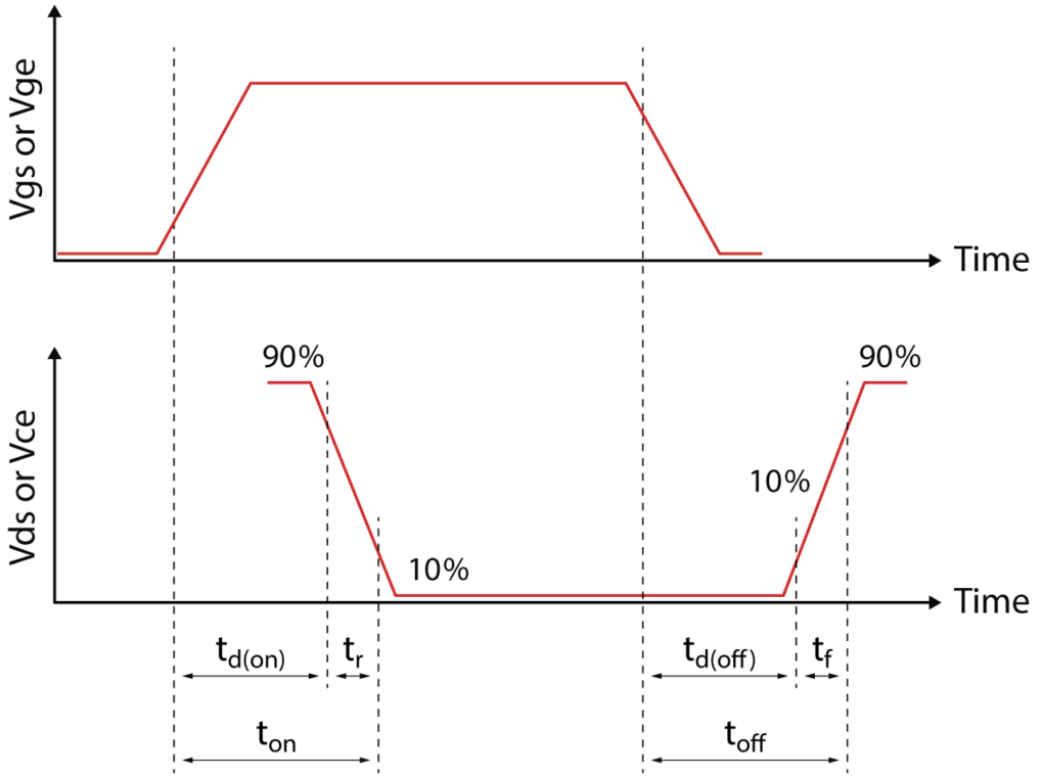
Part 4 – Power semiconductors

As shown in [1], the turn-on/turn-off asymmetry of power semiconductors can be computed with the following formula:

$$T_4 = (T_{d,\text{off}} + T_f) - (T_{d,\text{on}} + T_r)$$

With the following parameters:

- $T_{d,off}$: the turn-off time;
- T_f : the fall time;
- $T_{d,on}$: the turn-on time;
- T_r : the rise time.



Switching delays of a power semiconductor

The manufacturers of semiconductors always provide these parameters somehow in the datasheets, but at specific conditions. However, the switching characteristics are significantly impacted by the operating conditions V_{ds} and I_{ds} for MOSFETs (respectively V_{ce} and I_{ce} for IGBTs) as well as temperature.

Overall, it is therefore always wise to measure the switching characteristics in relevant operating conditions, whenever possible. However, as it is not always

technically feasible to measure the related timings – notably due to the difficult measurement of the drain/collector current – some approximations and some safety margin are always needed. For such cases, the table below provides the maximal turn-off/turn-on asymmetry T_4 for each power module and for specific operating conditions:

Power module	Semiconductor type	Operating conditions	T_4 [ns]
PEB8032 (discontinued)	Silicon IGBT	700V, 32A, R_G=10Ohm	380
PEB8024	Silicon carbide MOSFET	750V, 20A, R_G=2.5Ohm	20
PEB8038	Silicon carbide MOSFET	750V, 38A, R_G=30Ohm	270
PEB4050	Silicon IGBT	400V, 50A, R_G=10Ohm	100
PEB4046 (discontinued)	Silicon IGBT	400V, 46A, R_G=10Ohm	550
PEH4010	Silicon IGBT	400V, 10A, R_G=13Ohm	150
PEH2015	Silicon IGBT	200V, 15A, R_G=13Ohm	150
PEN8018	Silicon IGBT	700V, 15A, R_G=10Ohm	340

The above-reported timings, as well as the design procedure, are given here as a recommendation. They correspond to fully-tested parameters, which are proven effective in a broad variety of applications, but which are also likely to be sub-optimal in numerous cases. Ultimately, **only the user is responsible** for the selection of the most appropriate dead time for a given application.

Minimum dead time computation example

The proposed example is a B-Box RCP controlling a boost-type DC/DC converter made of one PEB8024. Following the above-presented design procedure, the minimum dead time is:

$$DT_{min} = (T_1 + T_2 + T_3 + T_4) \cdot 1.2 = (13 + 13 + 32 + 20) \cdot 1.2 = 94\,\text{ns}$$

Going further with dead time selection

Dependence of dead time on operating conditions

The above-presented design procedure reveals that, in most cases, the switching dynamics of the power semiconductors are the most important criteria for the selection of the dead time value. In particular, among the 4 corresponding timings, $T_{d,off}$ is the most influential.

On the other hand, $T_{d,off}$ is also the most impacted by the operating conditions, notably by the effective impedance seen from the collector/drain. In this regard, the following remarks can be made:

- Due to their low parasitic output capacitance, SiC MOSFETS are particularly sensitive to the load impedance. This phenomenon is highlighted in [3], which reports a **fivefold** augmentation of the complete turn-off time in a motor drive application. The article notably challenges the usual assumption regarding the (usually idealized) inductive nature of the load, which is here reaching its limits.
- The same authors also report in [4] that the switching trajectory in the V_{DS}·I_D plane may vary significantly, including cases where the drain current is so small that the usual switching dynamics no longer apply. Regarding shoot-through however, it seems that the prolonged rise time of the drain voltage doesn't require extending the dead time, as the current-related dynamics seem rather faster than in nominal operating conditions.
- While the proposed dead time selection procedure assumes here that one switch must have entirely turned off before the complementary switch may be turned on, it is sometimes possible to accept that a limited current circulates between both switches, contributing to speed up the switching process at light load. This, however, cannot be easily adjusted in a standard configuration.

Dead time compensation techniques

The introduction of a dead time unavoidably impacts the average output voltage. Depending on the current direction, the resulting voltage may be lower or higher than the desired voltage. This phenomenon is all the more important when the dead time is long compared to the switching period.

Nevertheless, since the impact on the produced average voltage can be anticipated, it can be compensated by software.

Dynamic dead time optimization

As the system efficiency is often negatively impacted by dead time, it may be worth optimizing the dead time during **run-time**, as a function of the operating conditions. For instance, authors of [4] report that the overall power losses can be reduced by up to 18% using such a technique.

Pragmatically, some improvements are also certainly already achievable using a dead-time that is “only” a function of the load current (which is often an already-available measurement). This could typically be implemented using a look-up table.

References

[1] Infineon, “Application Note AN2007-04: How to calculate and minimize the dead time requirement for IGBTs properly”, on Infineon website, May 2007.

[2] J. Lutz, H. Schlangenotto, U. Scheuermann and R. De Doncker, “Semiconductor Power Devices – Physics, Characteristics, Reliability,” Springer, 2011. (e-ISBN 978-3-642-11125-9)

[3] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock and D. J. Costinett, “Evaluation of Switching Performance of SiC Devices in PWM Inverter-Fed Induction Motor Drives,” in IEEE Trans. on Power Elect., Oct. 2015.

[4] Z. Zhang, H. Lu, D. J. Costinett, F. Wang, L. M. Tolbert and B. J. Blalock, “Model-Based Dead Time Optimization for Voltage-Source Converters Utilizing Silicon Carbide Semiconductors,” in IEEE Trans. on Power Elect., Nov. 2017.