MMC bundle - quick start guide

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This page explains how to get started with the modular multilevel converter (MMC) bundle configured as a 9-level, 3-phase inverter. It provides a comprehensive overview of the hardware configuration and step-by-step instructions to commission the equipment.

This page focuses on the basic commissioning of the default configuration of the **MMC bundle** (Figure 2), which is a 3-phase inverter containing 24 half-bridge submodules (Figure 1). For the sake of simplicity, the proposed commissioning plan uses an open-loop approach with **Sort-&-Select balancing**. This PWM-based modulation scheme inherently handles the balancing of the submodule voltages by sorting them and then selecting which module should be inserted or bypassed first. For more details on the implementation of the Sort-&-Select modulation, please refer to the technical note SS-PWM. Alternatively, a more advanced balancing strategy controlling all state variables is detailed in the technical note TN153.

Setting up the MMC bundle

The content of the MMC bundle, listed below, includes all the components needed for the realization of a 9-level, 3-phase inverter with 24 submodules.

- 3x programmable controllers (B-Box RCP)
- ACG SDK toolbox for automated generation of the controller code from Simulink or PLECS
- 3x power racks (type B)
- 24x full-bridge modules (PEH2015)
- 1x grid connection panel with switchgear and precharge circuit
- 4x voltage sensors
- 6x current sensors
- All necessary RJ45 and fiber optic cables

On top of that, some additional material, listed below, is required to test the system before operating the full converter.

- Laboratory DC power supply (rated for at least 100V, 5A)
- 3x power resistors (5-100Ω) to emulate a load at the grid terminal

Wiring of the power and control stages

Per default, in the MMC bundle, the full-bridge modules PEH2015 are wired in such a way that only one half-bridge is used. This way, one B-Box RCP suffices to drive the 16 switches of an MMC phase-leg (16 optical PWM outputs). The bundle therefore includes 3 B-Box RCP to interface with the 3 phases of the converter.

While the master B-Box RCP (device #0) runs the control for all 3 phases, it only interfaces with phase A. On the other hand, the slaves act as I/O extensions to phase B (device #1) and phase C (device #2). As such, the CPU in a slave B-Box RCP does not run, only the FPGA is active (see Distributed Converter Control for more details).

The wiring of the RJ45 analog signal cables (red) and the optical PWM gate signals (blue) for the 3 B-Box RCP is shown in Figure 3 below. At the back, the 3 B-Box RCPs are connected through SFP+ cables (orange).

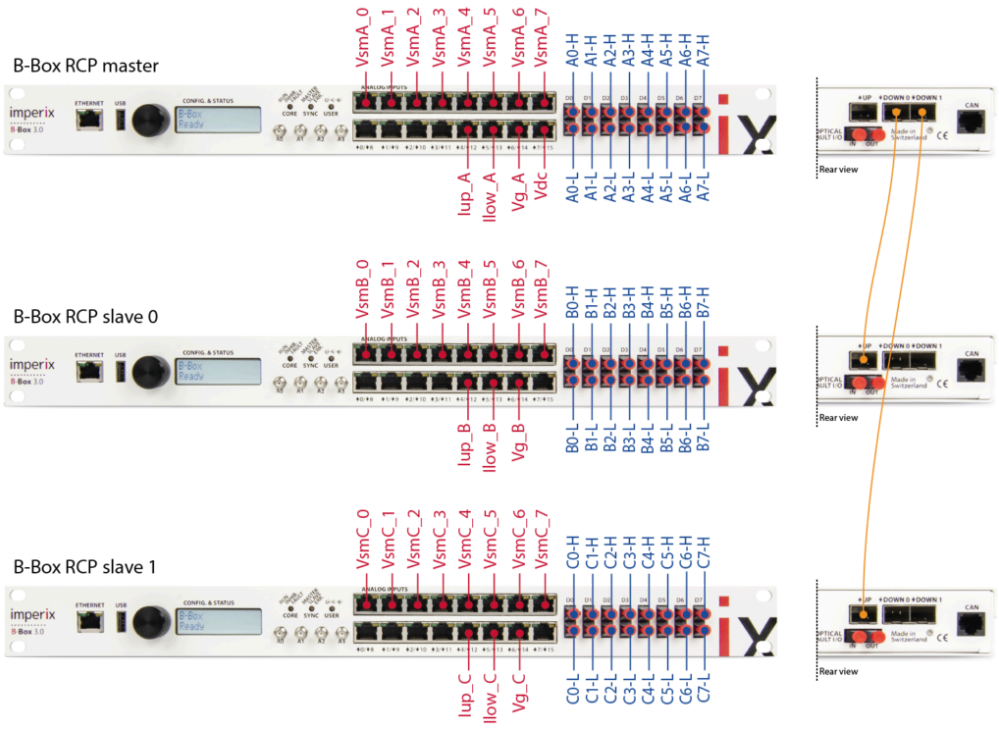

Figure 3: Signal wiring on the B-Box RCP

The counterpart of the wiring on the power racks is depicted in Figure 4.

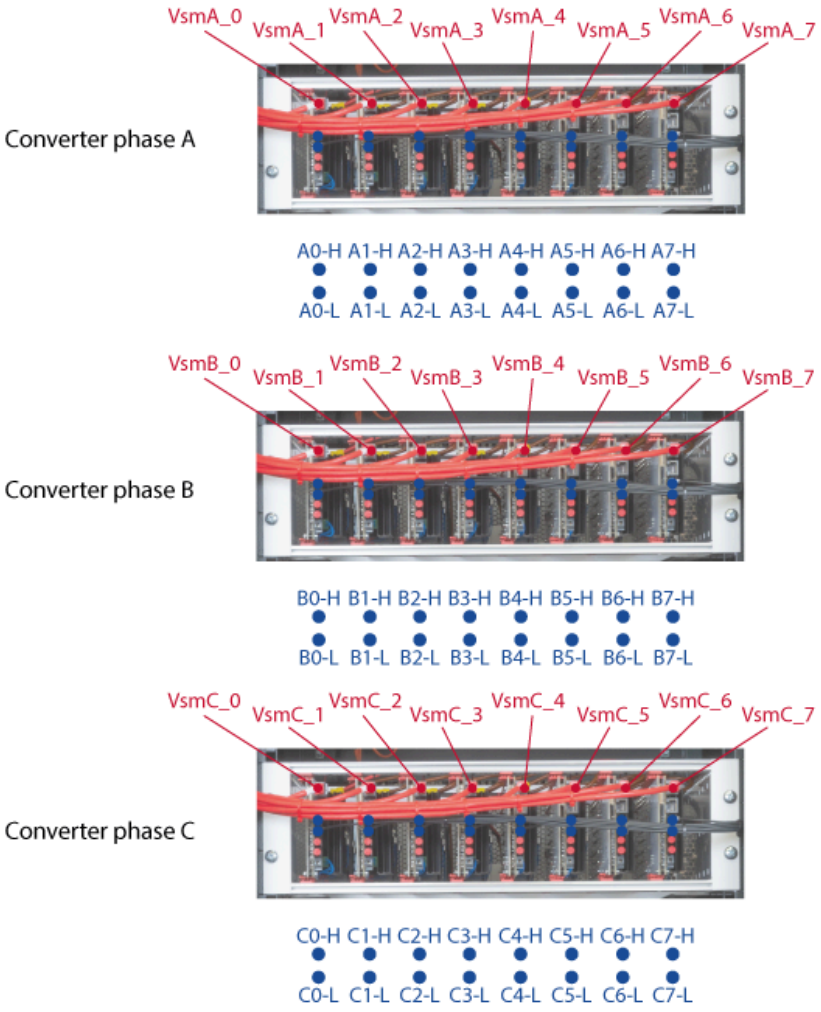

Figure 4: Signal wiring on the power racks

On the rear side of the cabinet, the power terminals, the grid connection panel, and the external voltage and current sensors are wired as shown in Figure 5.

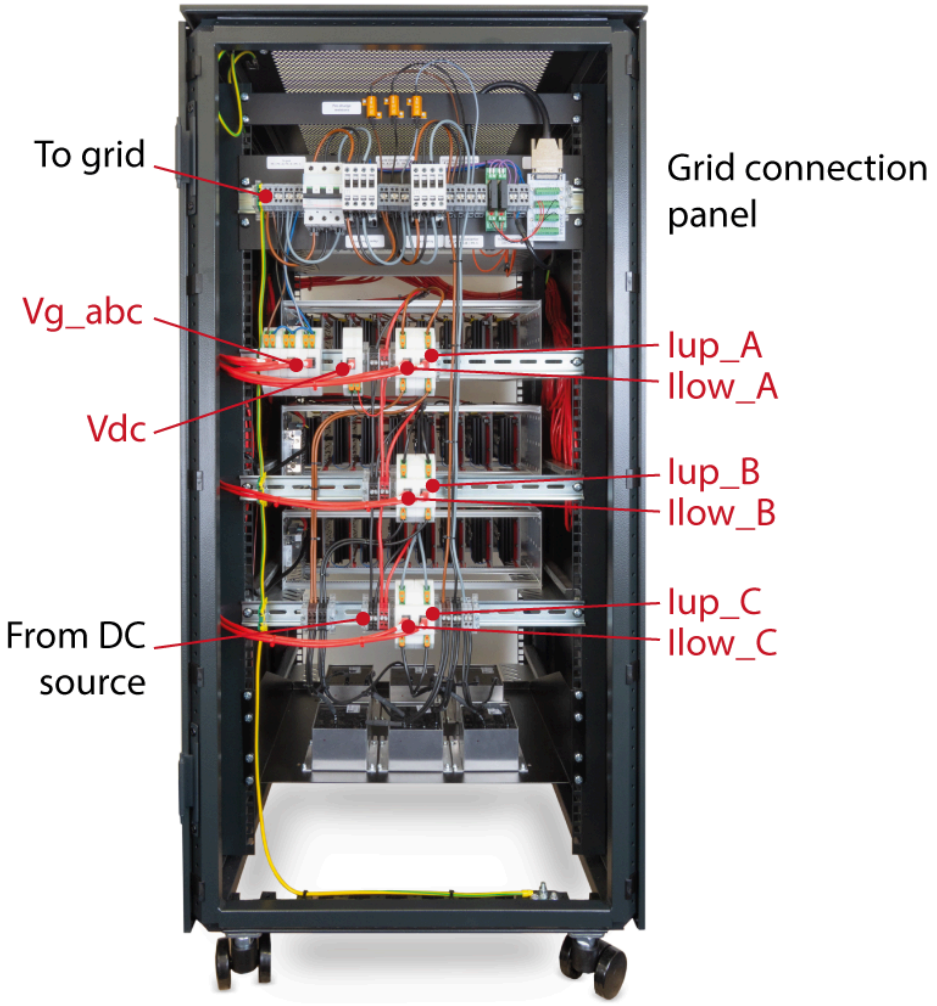

Figure 5: Rear view of the cabinet

Figure 6 gives a comprehensive overview of the electrical wiring as well as the naming of the measured signals and PWM gate signals.

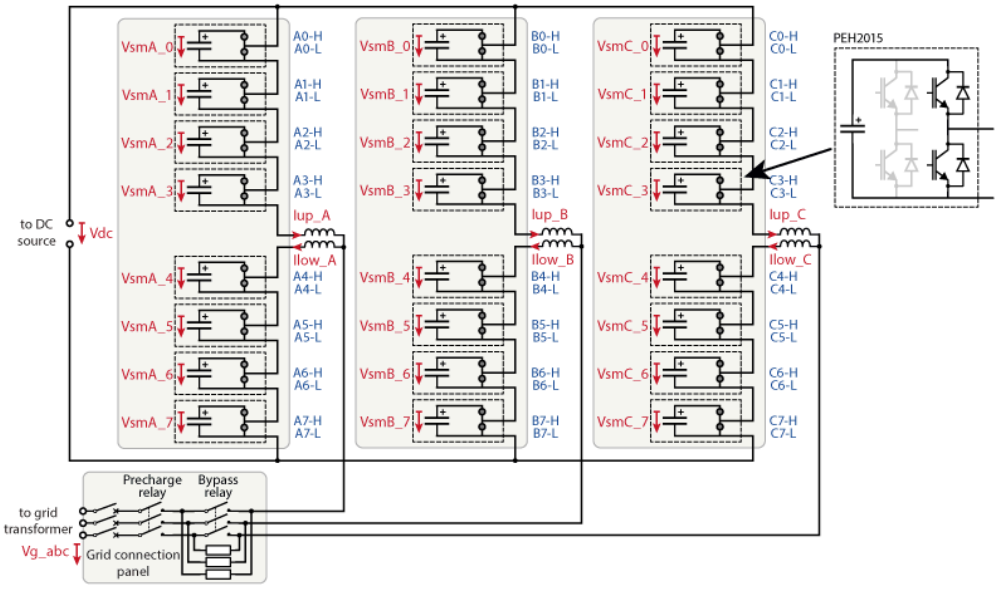

Figure 6: Overall system schematic including the measured signals (red) and PWM gate signals (blue).

Front panel configuration of the B-Box RCP

To ensure that the ratings of the power converter are never exceeded, the hardware protection limits of the B-Box RCP must be configured properly. A detailed explanation of how to compute these limits is given in PN105.

Measured signal	Range (SI units)	Sensor type	Input channel number	Low impedance	Gain	Filter	Limit high [V]	Limit low [V]	Disable safety
$V_{sm,(A,B,C),0...7}$	0… 220V	PEH2015 voltage	0…7	no	x4	no	7.1	-7.1	no
$I_{up,(A,B,C)}$	-15… 15A	DIN50A	12	no	x4	no	6	-6	no
$I_{low,(A,B,C)}$	-15… 15A	DIN50A	13	no	x4	no	6	-6	no
$V_{g,(A,B,C)}$	-335… 335V	DIN800V	14	no	x8	no	6.6	-6.6	no
V_{dc} (only on master B-Box)	0… 800 V	DIN800V	15	no	x4	no	7.9	-7.9	no

Table 1: Analog input configuration of the B-Box RCP

Commissioning the MMC bundle

Before operating the system, it is always a good idea to test that everything is properly wired and configured. With the help of the Simulink (or PLECS) model below, the following test procedure can be used to check the behavior of the MMC bundle wired as a 9-level, 3-phase inverter.

The B-Box controller can be programmed using Automated Code Generation (ACG) tools from Simulink and PLECS or directly in C++. In this section, the code examples are implemented with Simulink and PLECS. If you are not familiar with the code generation feature of Simulink or PLECS, please refer to the getting started with ACG SDK on Simulink or getting started with ACG SDK on PLECS. In any case, make sure to install the latest version of ACG SDK beforehand, available for download at imperix.com/downloads/.

Download **PN172_MMC_SSPWM_openLoop.zip**
Download **PN172_MMC_SSPWM_openLoop.plecs**

These basic models are designed to operate the boost converter and 3-phase inverter individually and in open loop. The ADC blocks retrieve the analog measurements for monitoring. The PWM blocks, along with the tunable parameters, send PWM signals with the desired duty cycle to the power converter. The relays of the grid-side panel are operated directly with tunable parameters.

Test procedure

An easy way to test an inverter is to operate it in open loop on a passive load. A DC power supply is connected to the DC input and three resistors in a star configuration are connected on the AC side of the converter, as shown in Figure 8 below.

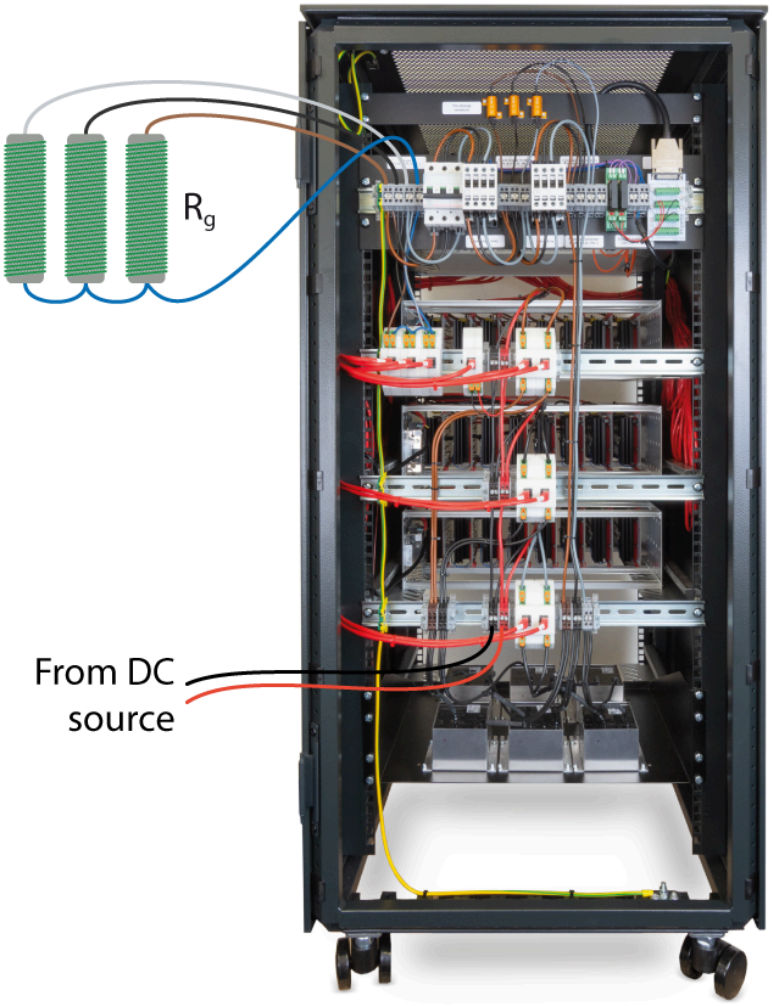

Figure 8: Converter wiring for the test: a DC power supply is connected to the DC input and a resistive load is connected in star at the grid terminal

Sizing of the load resistors

The resistors must be properly selected to prevent them from overheating. To do so, the expected RMS current through a resistor must not exceed its maximum rated current. The details of the computations are given hereafter.

The theoretical RMS current can be computed as

$$I_{g,rms} = \frac{\sqrt{2} \cdot V_{dc} \cdot M_{inv}}{2 \cdot R_g}$$

where V_{dc} is the DC input voltage, M_{inv} the modulation depth of the inverter (tunable parameter `M_inv`) and R_g the resistance of the load.
In this guide, R_g is chosen as $8.5\,\Omega$, $M_{inv} = 0.3$ and $V_{dc} = 200\,\mathrm{V}$. This results in an RMS current of $5\,\mathrm{A}$ through the resistors, which is within the rated current of the selected resistors ($13.5\,\mathrm{A}$).
If the rating of the resistor is exceeded, the DC supply voltage and/or the modulation depth of the inverter can be reduced accordingly.

Loading the code and setting up the workspace in Cockpit

- In Simulink:
    1. Open the Simulink model and set the mode to *Automated Code Generation* in the *CONFIG* block.

    2. Build the model (Ctrl + B). It will automatically launch Cockpit.
- Or in PLECS:
    1. Open the PLECS model.
    2. Open the coder options (Ctrl + Alt + B) and click *Build* in the bottom right. It will automatically launch Cockpit.
- In Cockpit:
    1. Set the target IP in Cockpit and click on *Create* to generate a new project.
    2. Add a new **rolling plot** module. Click four times on the "+" icon in the bottom right such as to see 5 sub-plots. Drag-&-drop the variables `VsmA_0` to `VsmA_7` into the 1st sub-plot, the variables `VsmB_0` to `VsmB_7` into the 2nd sub-plot and `VsmC_0` to `VsmC_7` into the 3rd. The input voltage `Vdc` can be drag-&-dropped to the 4th sub-plot and the input current `Idc` to the 5th.
    3. Add a new **scope** module. Click twice on the "+" icon on the bottom right of the scope to add two additional sub-plots to the scope. Drag-&-drop the grid grid voltages `Vg_a`, `Vg_b` and `Vg_c` to the 1st sub-plot and the grid currents `Ig_a`, `Ig_b` and `Ig_c` to the 2nd sub-plot. The 3rd sub-plot can be used to monitor the inductor voltages `Ilow_A`, `Ilow_B`, `Ilow_C`, `Iup_A`, `Iup_B` and `Iup_C`.

Step-by-step test procedure

1. Gradually increase the voltage of the DC source from 0V to 200V (or to the voltage chosen in the sizing of the resistors).
2. Verify that the measured input voltage `Vdc` matches the voltage of the source.
3. Verify that the sub-modules get charged to one eighth of the input voltage (25V in the presented example).
4. Manually close the breaker on the grid-side panel and close the relays by setting the variables `bypass_relay` and `precharge_relay` to 1 in the variable list on the left-hand side in Cockpit.
5. Enable the PWM pulses by toggling the PWM switch at the top left corner in Cockpit.
6. Verify that the sub-module capacitor voltages jump to one fourth of the input voltage (50V in the presented example).
7. The grid voltages should have a sinusoidal form with theoretical amplitude

$$\langle \hat{V_g} \rangle = M_{inv} \cdot V_{dc} \quad (\approx 60\,\mathrm{V}).$$

8. The grid currents should have a sinusoidal form with a theoretical amplitude

$$\langle \hat{I_g} \rangle = \frac{M_{inv} \cdot V_{dc}}{R_g} \quad (\approx 7\,\mathrm{A}).$$

9. The current drawn from the DC source should theoretically be

$$I_{dc} = \frac{3}{2} \cdot \frac{M_{inv}^2 \cdot V_{dc}}{R_g} \quad (\approx 3\,\mathrm{A}).$$

10. Reduce the input voltage to 0V and observe the discharging of the sub-module capacitors.
11. Disable the PWM.

The measured signals in this basic test are low compared to the measurement range of the sensors. Therefore, offsets in the range of $\pm 1\,\mathrm{V}$ and $\pm 0.5\,\mathrm{A}$ can be observed. Moreover, due to the non-idealities of the semiconductor switches (voltage drops, switching delays and dead-time), the grid voltage amplitude can be up to $10\,\mathrm{V}$ lower than the value computed above. Accordingly, the grid current amplitude can be up to $\frac{10\,\mathrm{V}}{R_g}$ lower than the theoretical value.
Due to the simplicity and open-loop nature of the proposed example code, limits might be reached if the PWM is enabled when the submodule capacitor voltages differ too much from each other, or in

case the sum of the capacitor voltages in one arm differs too much from Vdc. In these cases, the converter may trip and the fault must be acknowledged using the B-Box RCP front panel, as detailed in Programming Imperix Controllers.

The screenshot below shows how the workspace could look in the end, while running the test procedure.

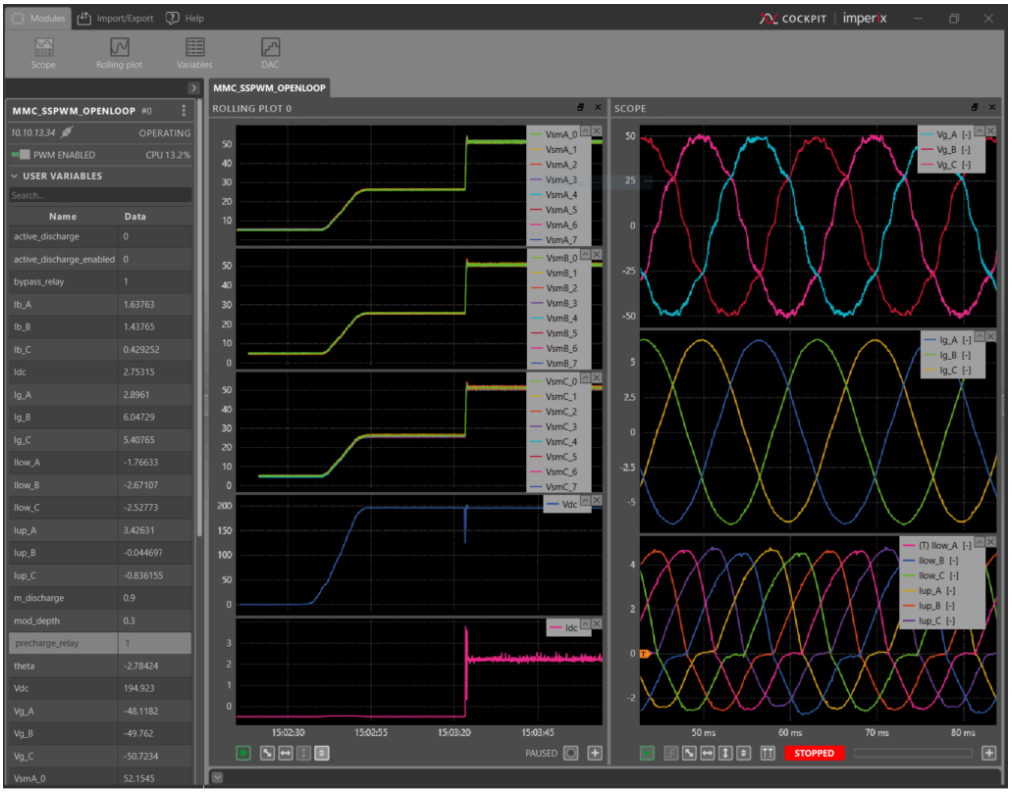

Figure 9: Running the test using Cockpit

To go further…

With the basic functionality of the equipment tested, one could dive deeper into the control strategy for the MMC, including its connection to the grid: Three-phase MMC converter. Another application using the MMC bundle is presented in MMC-based audio amplifier.

Other examples with modular multi-level topologies include the cascaded H-bridge (TN165), which can be applied for instance in solid-state transformers (AN015).