PEB – Half-bridge module

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Table of Contents

The PEB block is a simulation model included in the Imperix Power library. It models the imperix half-bridge module PEB8038, PEB8024, and PEB4050 in Simulink and PLECS simulation. For more information regarding the Imperix Power library, please read PN150.

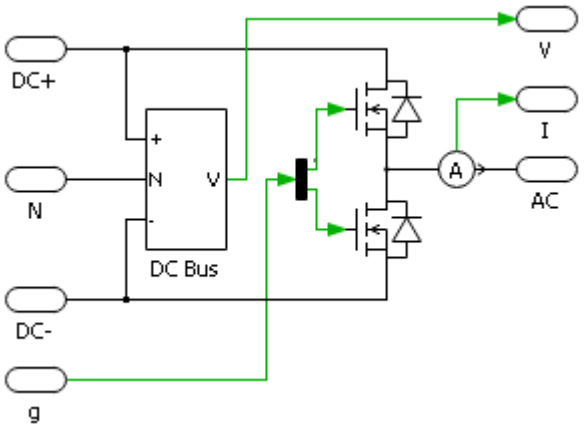
This block also provides thermal models for PEB8038 and PEB8024 (PEB4050 is currently unavailable). For more information regarding thermal simulation with the Imperix Power library, please read PN132.

Imperix Power library is available starting from ACG SDK 2024.2. Moreover, thermal simulation is enabled from ACG SDK 2025.1 BETA. Simulink Simscape Electrical or PLECS is also required. The Simulink version is only compatible with Specialized Power Systems. The supported versions are:
• Simulink R2016a or newer.
• Plexim PLECS 4.5 or newer.

Electrical modeling of PEB

The schematic of the electrical model of PEB is depicted on the right. It has two modeling levels:

- **(A) Simple**
- **(B) Detailed**

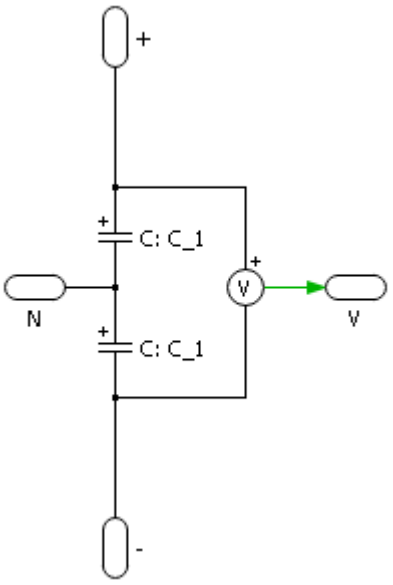


Schematic of PEB electrical model

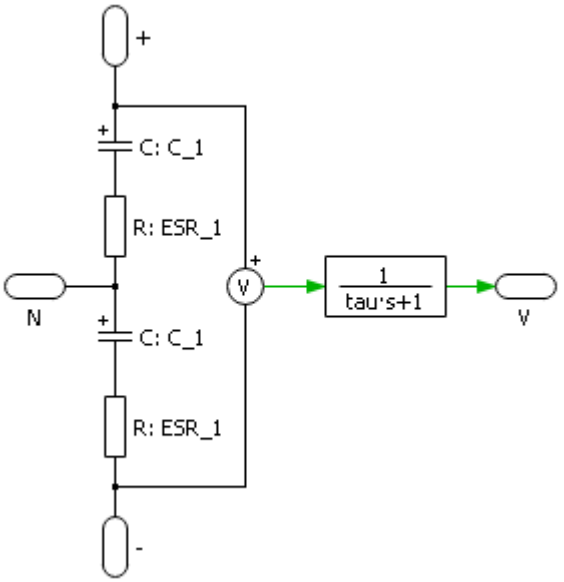
For more detailed model parameters and measurement results, please contact .

DC bus

The schematic of the equivalent DC bus is shown below.

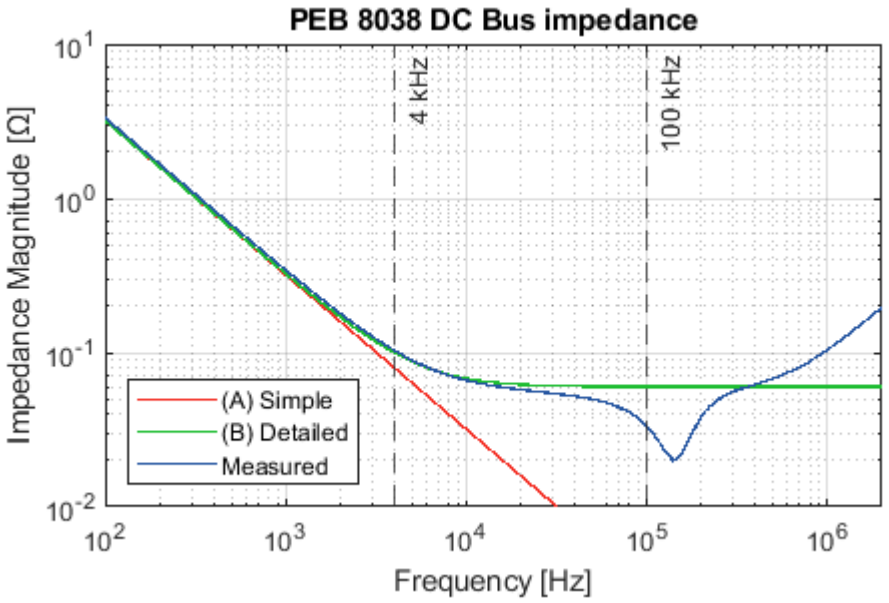


(A) Simple



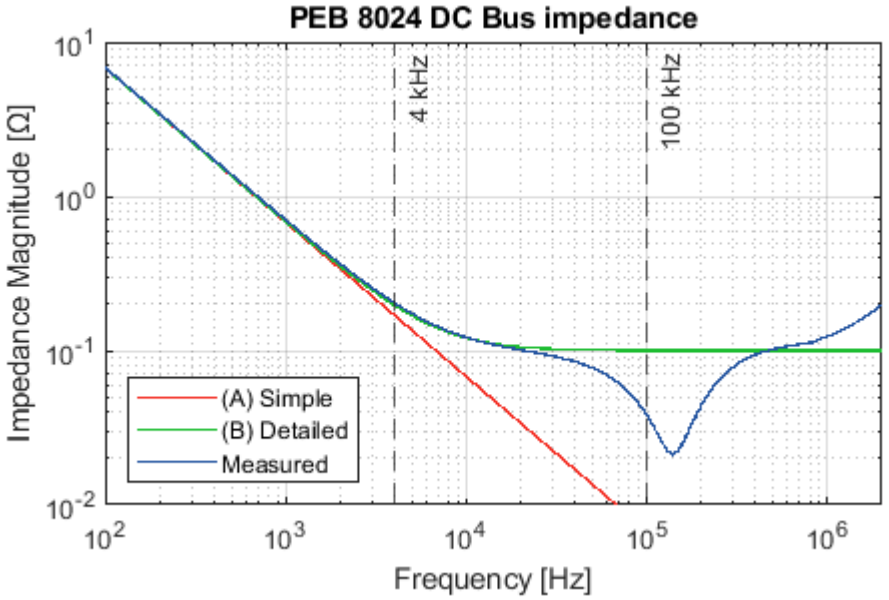
(B) Detailed

The simulation model is relevant within a given frequency range. The frequency validity range is 0-4 kHz for the (A) Simple level and 0-100 kHz for the (B) Detailed level. In that range, the impedance and transfer function of the model are reasonably close to the modeled system, which can be seen along with the plots of the proposed models. The model parameters are also displayed below.



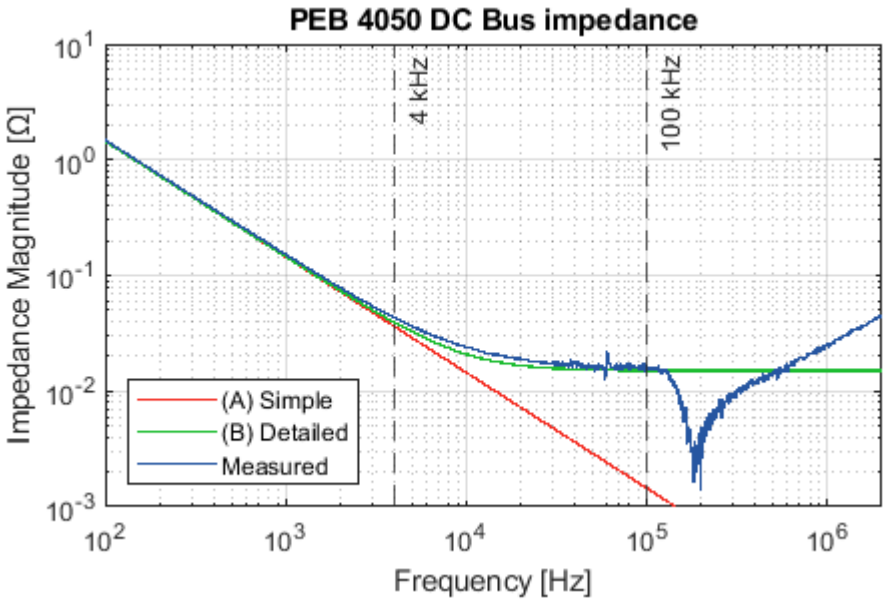
	C_1 [uF]	ESR_1 [mΩ]
(A)	500*2	0
(B)	500*2	60/2

Model Parameters of PEB8038



	C_1 [uF]	ESR_1 [mΩ]
(A)	235*2	0
(B)	235*2	110/2

Model Parameters of PEB8024

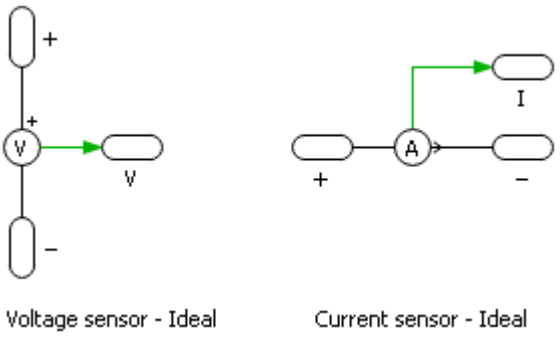


	C_1 [uF]	ESR_1 [mΩ]
(A)	1100*2	0
(B)	1100*2	15/2

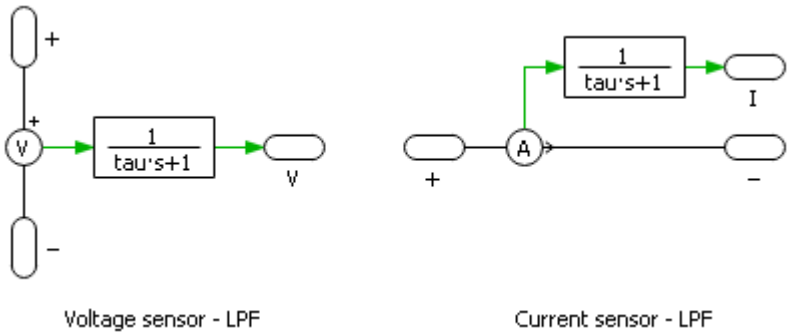
Model Parameters of PEB4050

Embedded sensors

A generic sensor can be approximately modeled by an ideal sensor in series with an optional first-order Low-Pass Filter (LPF). The relationship between sensor's bandwidth f_{BW} and the time constant τ of the LPF follows $\tau = \frac{1}{2\pi f_{BW}}$.



Ideal model



1st-order LPF model

A sensor is modeled as a first-order LPF only if its bandwidth lies within the frequency range of a given modeling level. Otherwise, it is modeled as an ideal sensor. The following table summarizes the information on all the sensors in the PEB.

Sensor	Bandwidth [kHz]	(A) Simple	(B) Detailed
PEB voltage sensor	8	Ideal	LPF
PEB current sensor	280	Ideal	Ideal

Modeling of the sensors in PEB

Power transistors

The PEB block offers two options for modeling the power transistors:

- **Switched** The transistors are modeled by individual power semiconductors. The control inputs are instantaneous logical gate signals.
- **Averaged** The transistors are modeled by controlled voltage and current sources. The control inputs are the relative on-times of the semiconductors with values between 0 and 1. The gate signals can be either instantaneous (using only values 0 and 1) or time-averaged.

Although the functionality is practically the same, these options are named differently in PLECS and Simulink Simscape to be consistent with their naming conventions.

In Simulink Simscape they are named:

- **Switching devices**
- **Switching function**

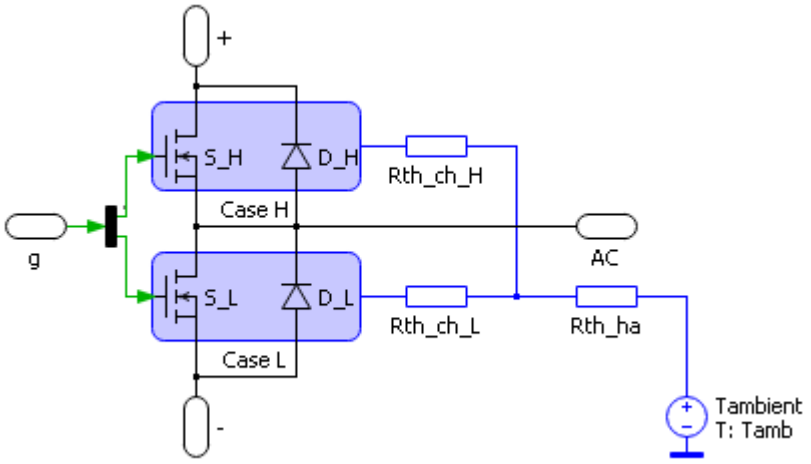
In PLECS they are named:

- **Switched**
- **Sub-cycle average**

Thermal modeling of PEB

The schematic of the thermal model of PEB8038 and PEB8024 is depicted on the right.

It includes the loss model of the semiconductors and the thermal impedance network between the junction and the ambient temperature.



Schematic of PEB thermal model

Thermal impedance network

The thermal impedance model models only the thermal resistances, and all the thermal capacitances are either ignored or fixed at a small value to reduce the simulation time for the system to reach a thermal steady state. The model parameters are displayed below. Note that the thermal impedance between the junction and the case is included in the transistor's thermal description file and thus is not present in the schematic above.

Thermal resistance	Value [K/W]
MOSFET junction to case resistance	0.2755
Diode junction to case resistance	0.2755
Case to Heatsink resistance Rth_ch	0.406
Heatsink to ambient temperature resistance Rth_ha	0.2839

Thermal impedance model parameters of PEB8038

Thermal resistance	Value [K/W]
MOSFET junction to case resistance	0.6466
Diode junction to case resistance	0.6466
Case to Heatsink resistance Rth_ch	0.41
Heatsink to ambient temperature resistance Rth_ha	0.3463

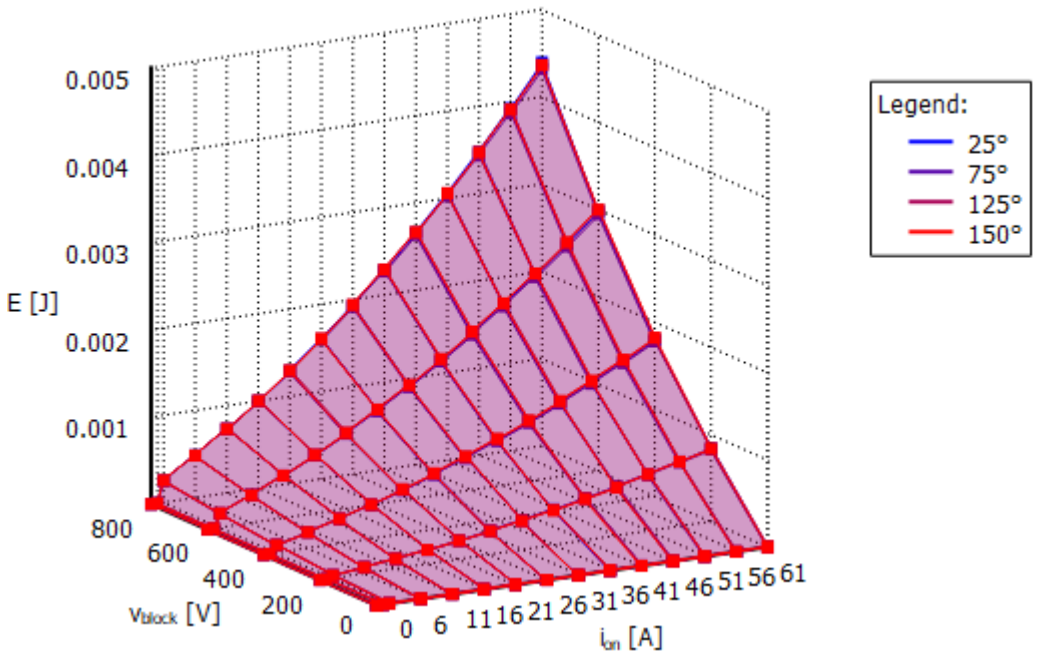
Thermal impedance model parameters of PEB8024

Semiconductor loss model

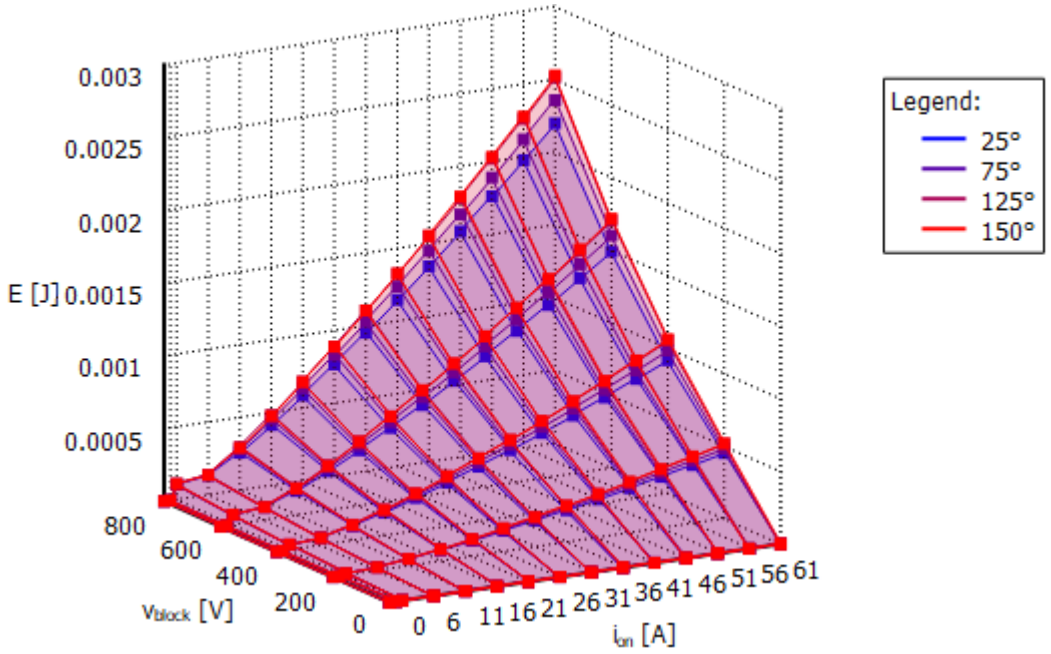
The semiconductor's turn-on loss E_{on}, turn-off loss E_{off}, and on-state drain-to-source voltage V_{on} are modeled by look-up-tables provided by manufacturers. The module's switching loss P_{sw} is calculated by periodic impulse averages of E_{on} and E_{off} over a chosen period, which is 1ms by default. The conduction loss P_{cond} is calculated by $P_{cond} = V_{on} \cdot I_{on}$. The detailed model implementation in Simulink and PLECS can be viewed in PN132, and the look-up-tables are provided below.

Look-up-tables of PEB8038

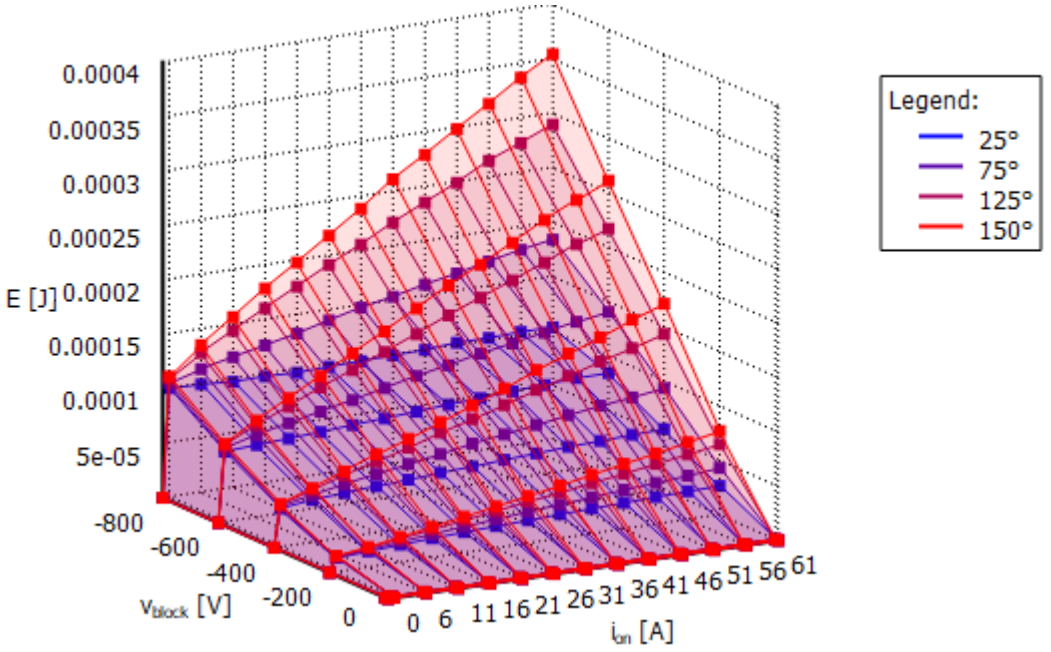
The look-up-tables of the Onsemi NTHL020N120SC1 used in PEB8038 are shown below.



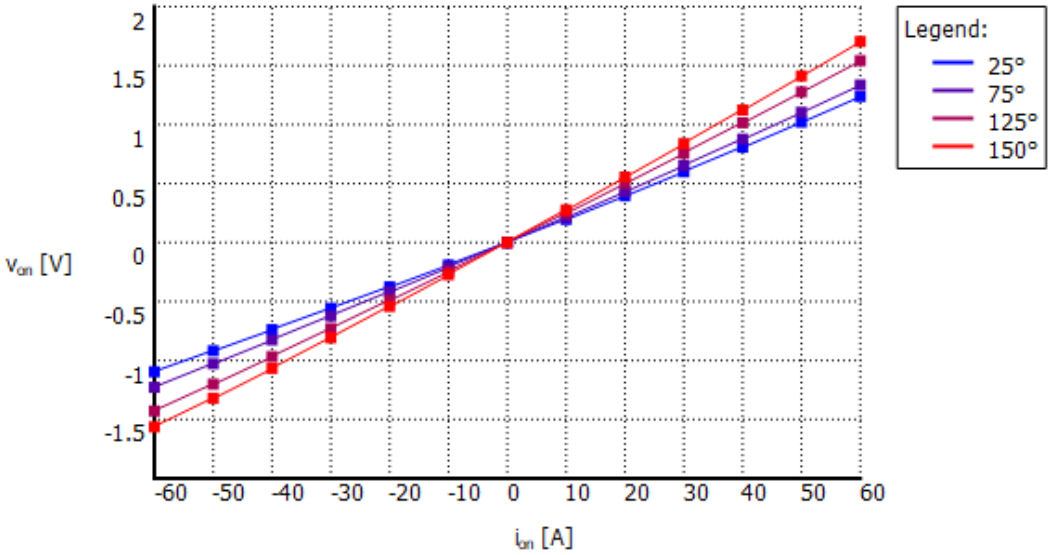
PEB8038 MOSFET Eon



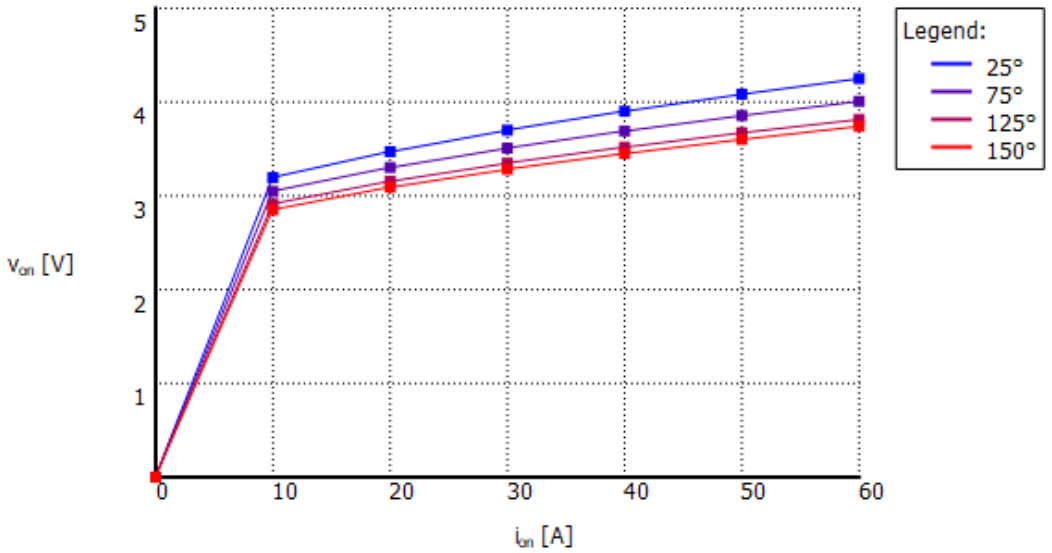
PEB8038 MOSFET Eoff



PEB8038 Diode Eoff



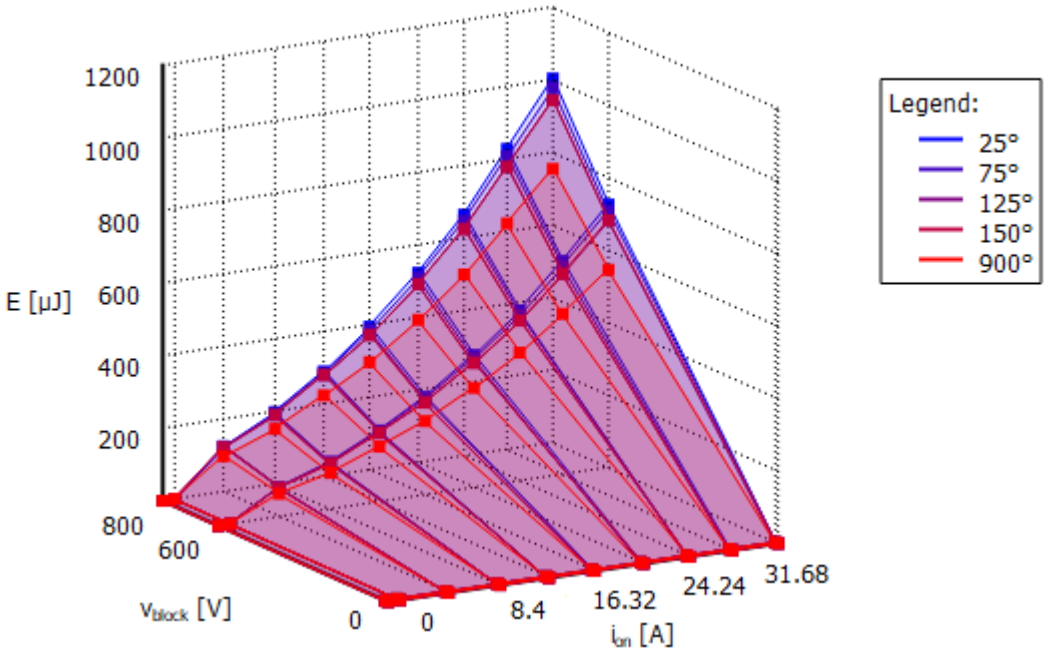
PEB8038 MOSFET Von



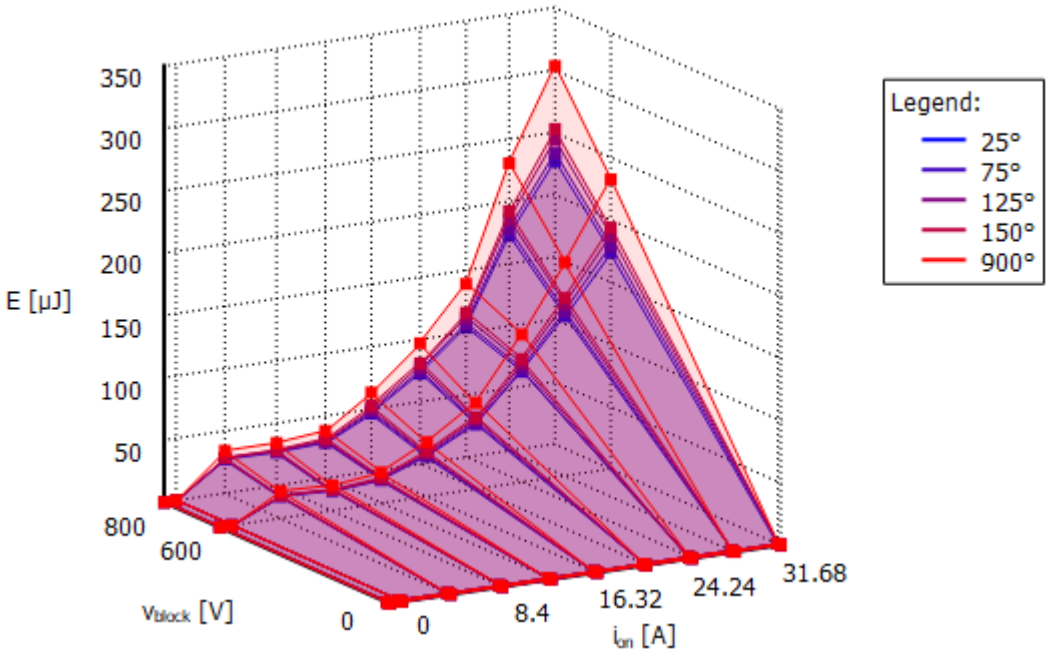
PEB8038 Diode Von

Look-up-tables of PEB8024

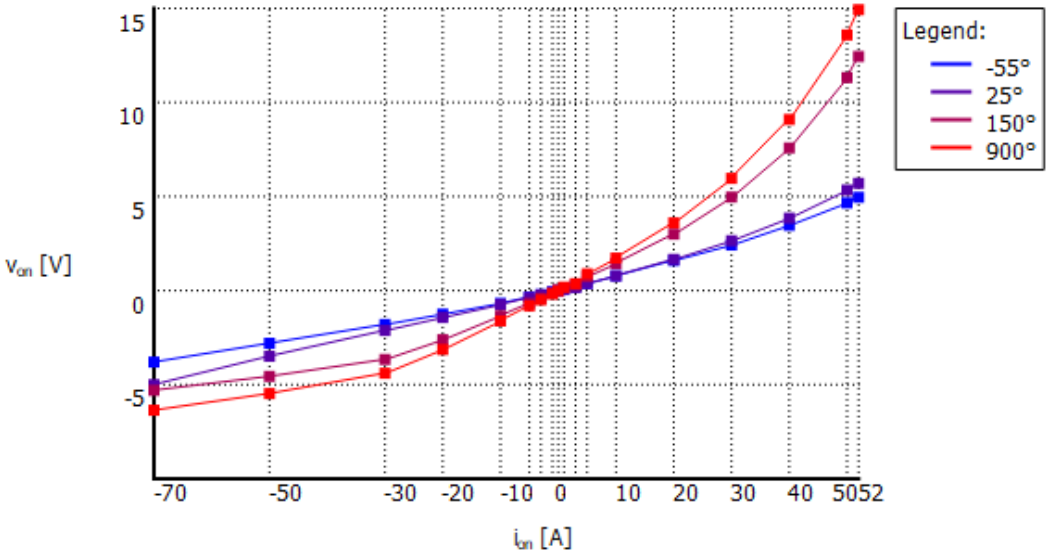
The look-up-tables of the Wolfspeed C2M0080120D used in PEB8024 are shown below. The turn-off loss of the body diode is merged with the turn-on loss of the MOSFET.



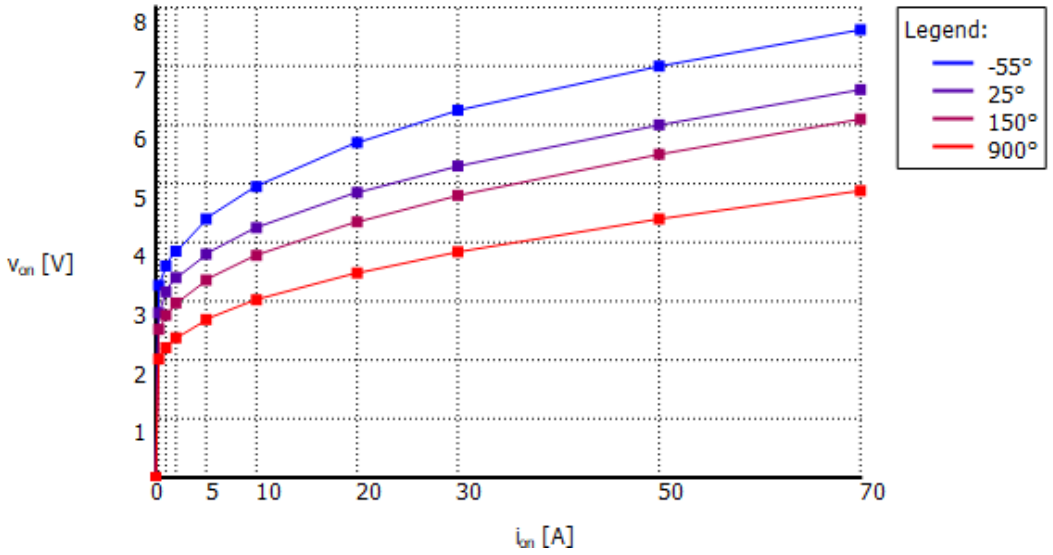
PEB8024 MOSFET Eon



PEB8024 MOSFET Eoff



PEB8024 MOSFET Von



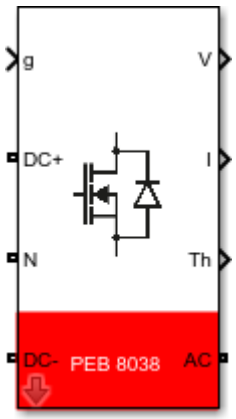
PEB8024 Diode Von

Simulink PEB block

Port specification

- The input g is the gate signal. It has a width of 2, representing the signals for the high and low gates.
    - For `Switching devices (switched)` model, g is the 0/1 PWM signal.
    - For `Switching Function (averaged)` model, g can be either the 0/1 PWM signal or the duty cycle between 0 and 1.
- The output `V` is the measured voltage across the DC bus.
- The output `I` is the measured output current.

- The output `Th` is the thermal simulation results. This port is only visible when thermal simulation is enabled.
- The connection port `DC+` is the electrical port connected to the positive pole of the DC bus.
- The connection port `DC-` is the electrical port connected to the negative pole of the DC bus.
- The connection port `N` is the electrical port connected to the midpoint of the DC bus.
- The connection port `AC` is the electrical port connected to the AC output.

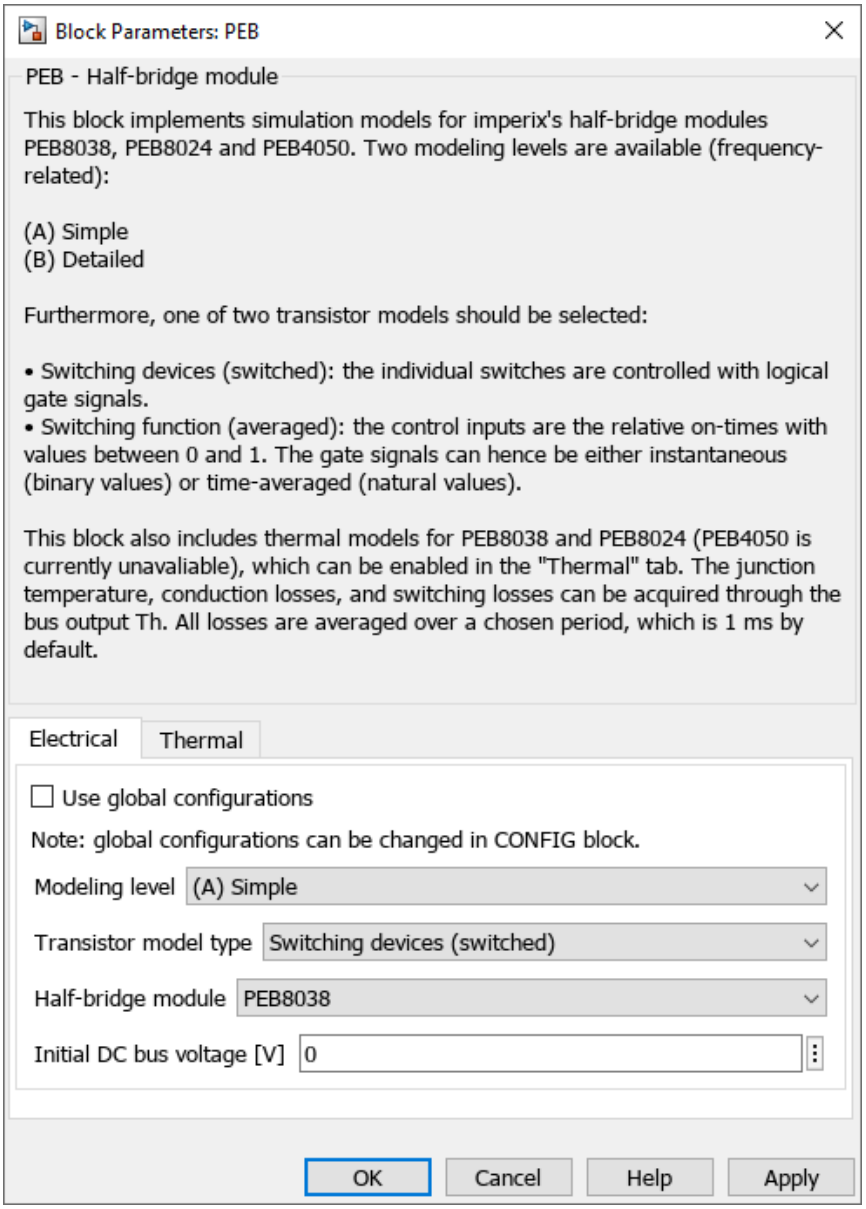


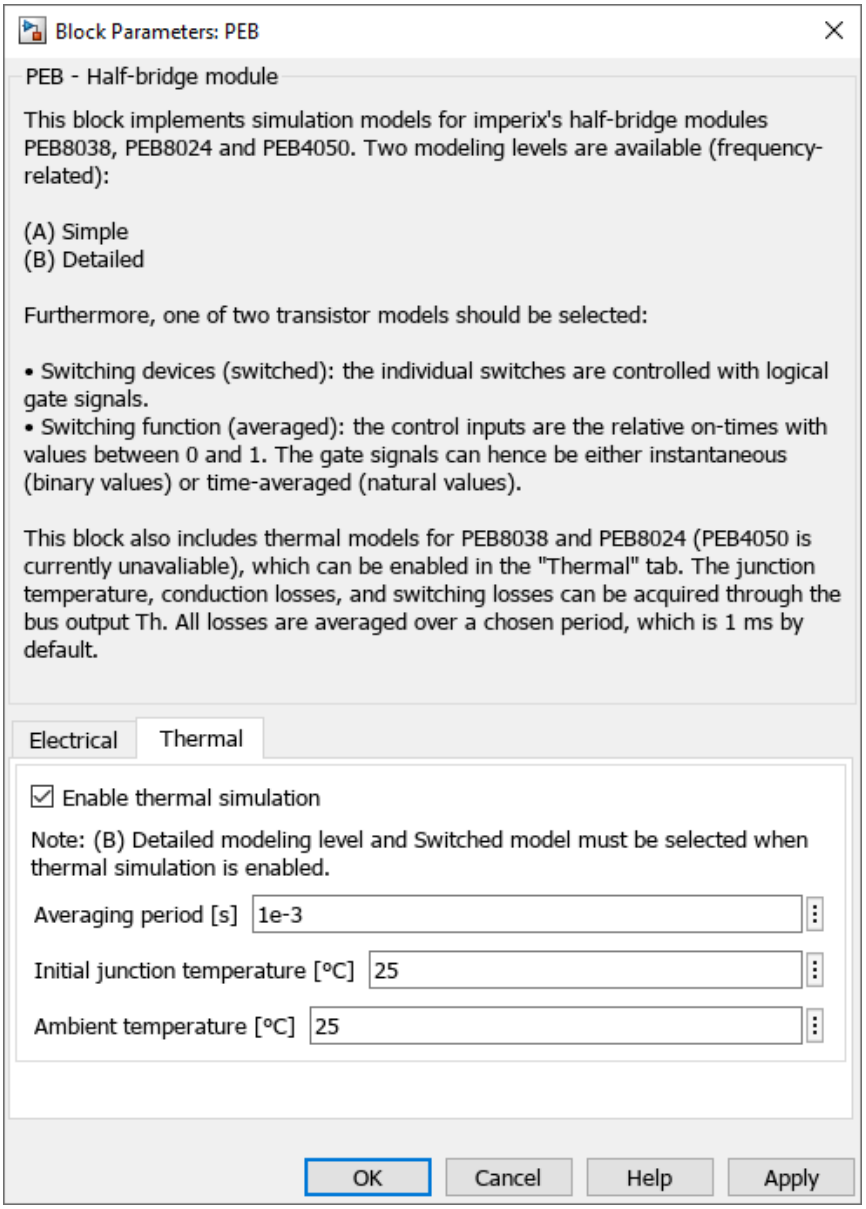
Electrical parameters

- `Use global configurations` is ticked when the block receives global configurations from the `Config` block.
- `Modeling level` selects the modeling level of the peripheral circuits.
- `Transistor model type` selects the model of the power transistors.
- `Half-bridge module` selects the type of PEB products to be simulated.
- `Initial DC bus voltage [V]` defines the initial voltage across the DC bus when the simulation starts.

Thermal parameters

- `Enable thermal simulation` is ticked when the thermal simulation is enabled.
- `Averaging period [s]` defines the averaging period for calculating switching loss.
- `Initial junction temperature [°C]` defines the initial junction temperature when the simulation starts.
- `Ambient temperature [°C]` defines the ambient temperature throughout the simulation.


Block Parameters: PEB
PEB - Half-bridge module
This block implements simulation models for imperix's half-bridge modules PEB8038, PEB8024 and PEB4050. Two modeling levels are available (frequency-related):
(A) Simple
(B) Detailed
Furthermore, one of two transistor models should be selected:
• Switching devices (switched): the individual switches are controlled with logical gate signals.
• Switching function (averaged): the control inputs are the relative on-times with values between 0 and 1. The gate signals can hence be either instantaneous (binary values) or time-averaged (natural values).
This block also includes thermal models for PEB8038 and PEB8024 (PEB4050 is currently unavaliable), which can be enabled in the "Thermal" tab. The junction temperature, conduction losses, and switching losses can be acquired through the bus output Th. All losses are averaged over a chosen period, which is 1 ms by default.
Electrical
Thermal
Use global configurations
Note: global configurations can be changed in CONFIG block.
Modeling level
(A) Simple
Transistor model type
Switching devices (switched)
Half-bridge module
PEB8038
Initial DC bus voltage [V]
0
OK
Cancel
Help
Apply

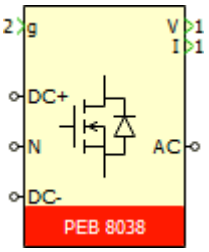


PLECS PEB block

Port specification

- The input g is the gate signal with a width of 2, representing the signals for the high and low gates.
    - For `Switched` model, g is the 0/1 PWM signal.
    - For `Sub-cycle average` model, g can be either the 0/1 PWM signal or the duty cycle between 0 and 1.
- The output `V` is the measured voltage across the DC bus.
- The output `I` is the measured output current.
- The connection port `DC+` is the electrical port connected to the positive pole of the DC bus.

- The connection port `DC-` is the electrical port connected to the negative pole of the DC bus.
- The connection port `N` is the electrical port connected to the midpoint of the DC bus.
- The connection port `AC` is the electrical port connected to the AC output.

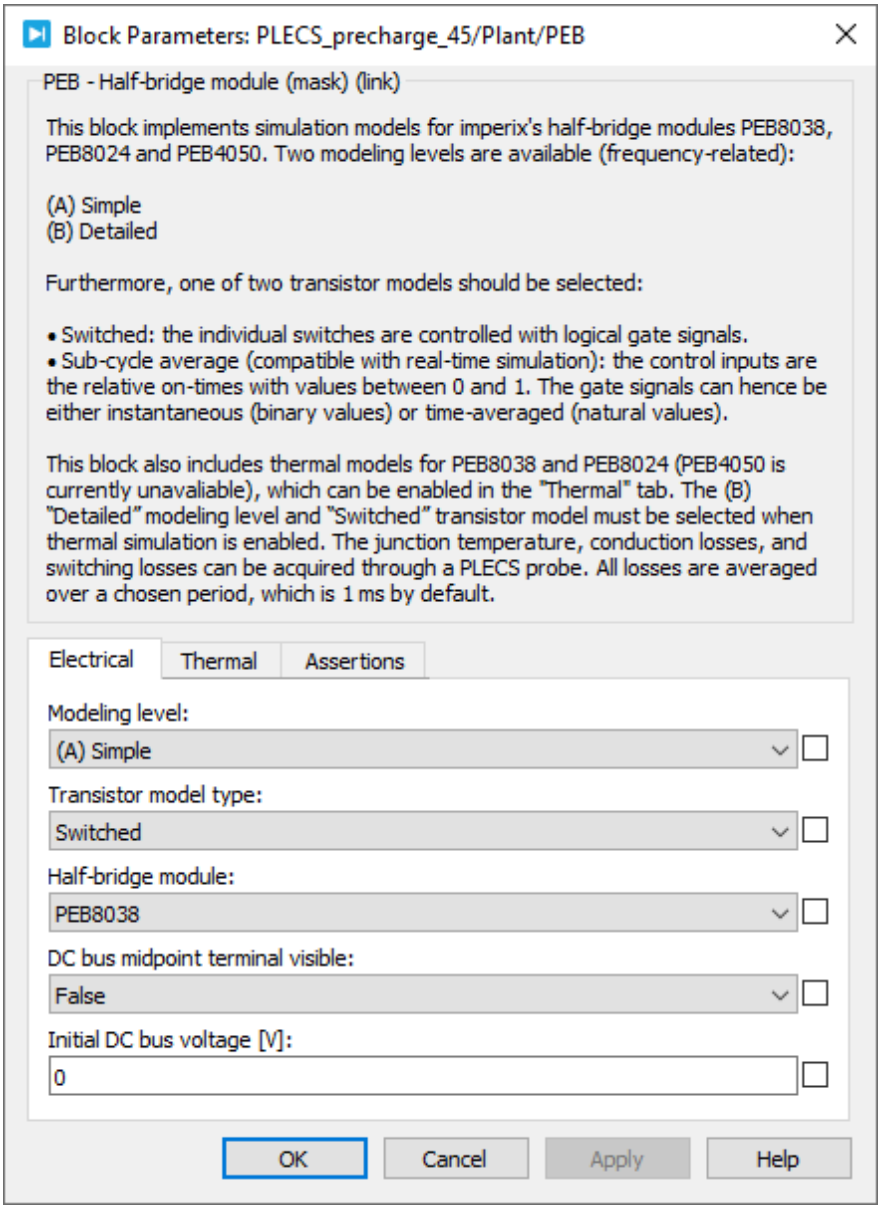


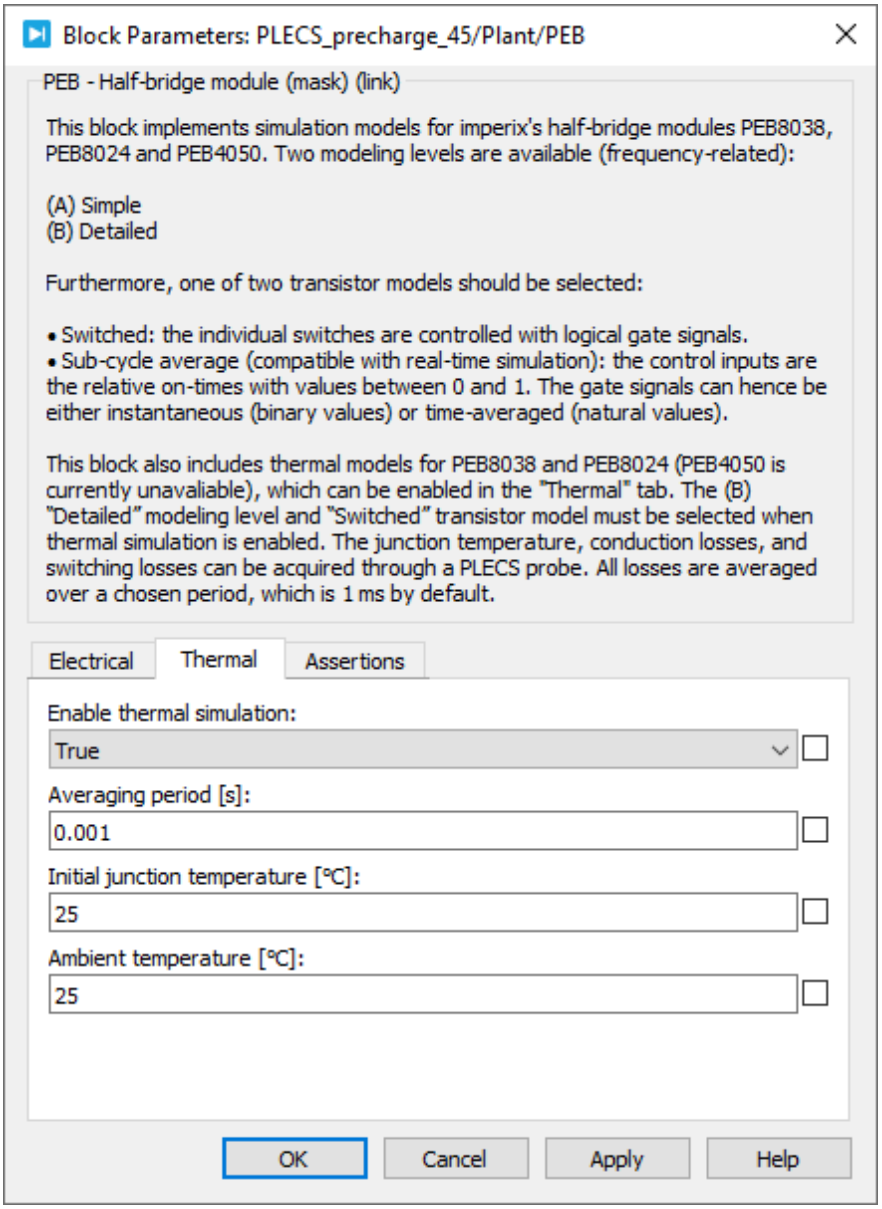
Electrical parameters

- `Modeling level` selects the modeling level of the peripheral circuits.
- `Transistor model type` selects the model of the power transistors.
- `Half-bridge module` selects the type of PEB products to be simulated.
- `DC Bus midpoint terminal visible` shows or hides the port `N`.
- `Initial DC bus voltage [V]` defines the initial voltage across the DC bus when the simulation starts.

Thermal parameters

- `Enable thermal simulation` is ticked when the thermal simulation is enabled.
- `Averaging period [s]` defines the averaging period for calculating switching loss.
- `Initial junction temperature [°C]` defines the initial junction temperature when the simulation starts.
- `Ambient temperature [°C]` defines the ambient temperature throughout the simulation.


Block Parameters: PLECS_precharge_45/Plant/PEB
PEB - Half-bridge module (mask) (link)
This block implements simulation models for imperix's half-bridge modules PEB8038, PEB8024 and PEB4050. Two modeling levels are available (frequency-related):
(A) Simple
(B) Detailed
Furthermore, one of two transistor models should be selected:
• Switched: the individual switches are controlled with logical gate signals.
• Sub-cycle average (compatible with real-time simulation): the control inputs are the relative on-times with values between 0 and 1. The gate signals can hence be either instantaneous (binary values) or time-averaged (natural values).
This block also includes thermal models for PEB8038 and PEB8024 (PEB4050 is currently unavaliable), which can be enabled in the "Thermal" tab. The (B) "Detailed" modeling level and "Switched" transistor model must be selected when thermal simulation is enabled. The junction temperature, conduction losses, and switching losses can be acquired through a PLECS probe. All losses are averaged over a chosen period, which is 1 ms by default.
Electrical
Thermal
Assertions
Modeling level:
(A) Simple
Transistor model type:
Switched
Half-bridge module:
PEB8038
DC bus midpoint terminal visible:
False
Initial DC bus voltage [V]:
0
OK
Cancel
Apply
Help



Probe signals

The following signals can be monitored by a Probe block in PLECS.

- `Gate signals` monitors the gate signals present at the input g.
- `DC Bus voltage true value [V]` monitors the true value of the DC bus voltage in Volt.
- `DC Bus voltage sensor output [V]` monitors the physical output of the DC bus voltage sensor in Volt.
- `Output current true value [A]` monitors the true value of the output current in Amp.
- `Output current sensor output [V]` monitors the physical output of the output current sensor in Volt.

The following signals contain thermal simulation results that can be monitored when thermal simulation is enabled.

- `Transistor H junction temperature [°C]` monitors the junction temperature of transistor H in °C.
- `Transistor L junction temperature [°C]` monitors the junction temperature of transistor L in °C.
- `Total conduction loss [W]` monitors the module's total conduction loss in Watt.
- `Total switching loss [W]` monitors the module's total switching loss in Watt.
- `Transistor H conduction loss [W]` monitors the conduction loss of transistor H in Watt.
- `Transistor L conduction loss [W]` monitors the conduction loss of transistor L in Watt.
- `Transistor H switching loss [W]` monitors the switching loss of transistor H in Watt.
- `Transistor L switching loss [W]` monitors the switching loss of transistor L in Watt.