PEH - Full-bridge module

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The PEH block is a simulation model included in the <u>Imperix Power library</u>. It models the imperix full-bridge module <u>PEH4010</u> and <u>PEH2015</u> in Simulink and PLECS simulation.

For more information regarding the Imperix Power library, please read <u>Getting</u> <u>started with Imperix Power library</u>.

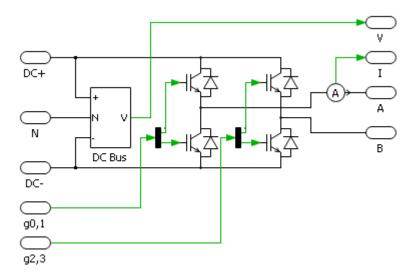
Imperix Power library is available starting from ACG SDK 2024.2. Simulink Simscape Electrical or PLECS is also required. The Simulink version is only compatible with Specialized Power Systems. The supported versions are:

- · Simulink R2016a or newer.
- Plexim PLECS 4.5 or newer.

Modeling of PEH

The schematic of the PEH model is depicted on the right. It has two modeling levels:

- (A) Simple
- (B) Detailed

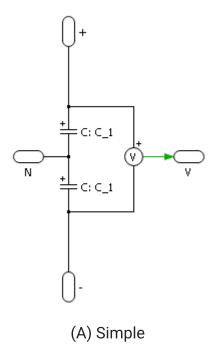


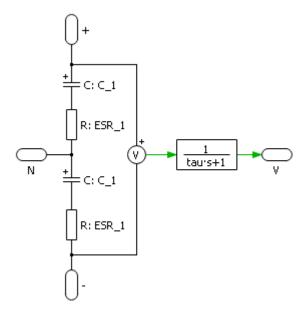
Schematic of PEH model

For more detailed model parameters and measurement results, please contact .

DC bus

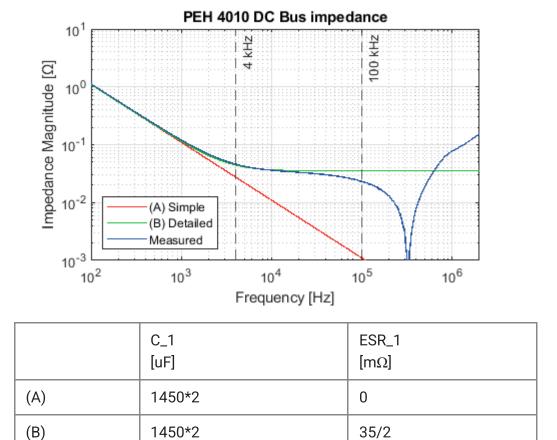
The schematic of the equivalent DC bus is shown below.



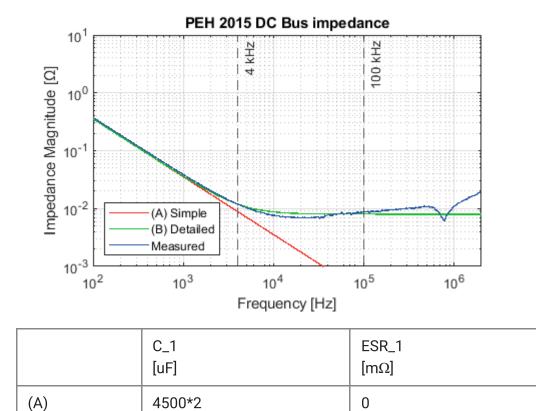


(B) Detailed

The simulation model is relevant within a given frequency range. The frequency validity range is 0-4 kHz for the (A) Simple level and 0-100 kHz for the (B) Detailed level. In that range, the impedance and transfer function of the model are reasonably close to the modeled system, which can be seen along with the plots of the proposed models. The model parameters are also displayed below.



Model Parameters of PEH4010



Model Parameters of PEH2015

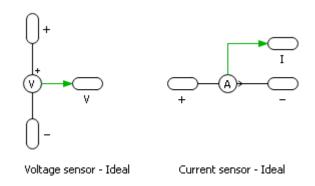
8/2

Embedded sensors

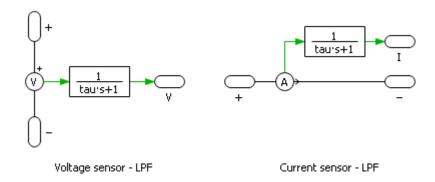
4500*2

(B)

A generic sensor can be approximately modeled by an ideal sensor in series with an optional first-order Low-Pass Filter (LPF). The relationship between sensor's bandwidth f_{BW} and the time constant τ of the LPF follows $\tau=\frac{1}{2\pi f_{BW}}$.



Ideal model



1st-order LPF model

A sensor is modeled as a first-order LPF only if its bandwidth lies within the frequency range of a given modeling level. Otherwise, it is modeled as an ideal sensor. The following table summarizes the information on all the sensors in the PEH.

Sensor	Bandwidth [kHz]	(A) Simple	(B) Detailed
PEH voltage sensor	25	Ideal	LPF
PEH current sensor	120	Ideal	Ideal

Modeling of the sensors in PEH

Power transistors

The PEH block offers two options for modeling the power transistors:

- **Switched** The transistors are modeled by individual power semiconductors. The control inputs are instantaneous logical gate signals.
- **Averaged** The transistors are modeled by controlled voltage and current sources. The control inputs are the relative on-times of the semiconductors with values between 0 and 1. The gate signals can be either instantaneous (using only values 0 and 1) or time-averaged.

Although the functionality is practically the same, these options are named differently in PLECS and Simulink Simscape to be consistent with their naming conventions.

In Simulink Simscape they are named:

- Switching devices
- Switching function

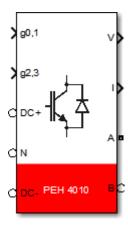
In PLECS they are named:

- Switched
- Sub-cycle average

Simulink PEH block

Port specification

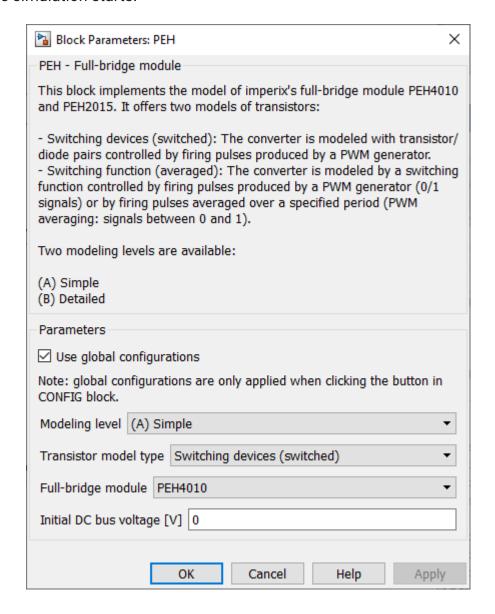
- The input g0,1 and g2,3 are the gate signals. There are 4 signals in total, and the order is shown in the schematic.
 - For Switching devices (switched) model, g0,1 and g2,3 are the 0/1 PWM signals.
 - For Switching Function (averaged) model, g0,1 and g2,3 can be
 either the 0/1 PWM signals or the duty cycles between 0 and 1.
- The output V is the measured voltage across the DC bus.
- The output I is the measured output current.
- The connection port DC+ is the electrical port connected to the positive pole of the DC bus.
- The connection port DC- is the electrical port connected to the negative pole of the DC bus.
- The connection port N is the electrical port connected to the midpoint of the DC bus
- The connection port A and B are the electrical ports connected to the AC output.



Parameters

- Use global configurations is ticked when the block receives global configurations from the Config block.
- Modeling level selects the modeling level of the peripheral circuits.
- Transistor model type selects the model of the power transistors.

- Full-bridge module selects the type of PEH products to be simulated.
- Initial DC voltage [V] defines the initial voltage across the DC bus when the simulation starts.

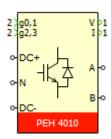


PLECS PEH block

Port specification

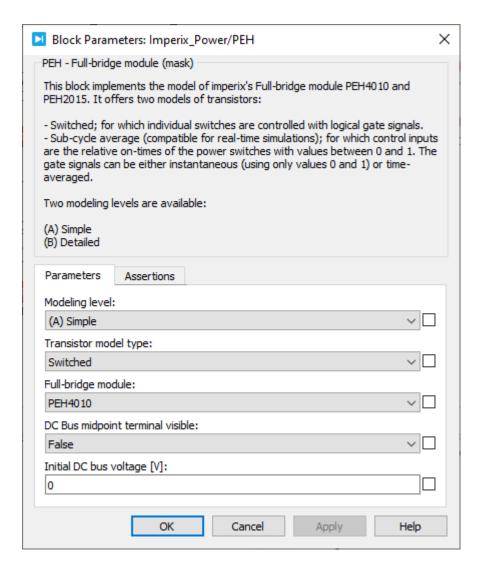
- The input g0,1 and g2,3 are the gate signals. There are 4 signals in total, and the order is shown in the schematic.
 - For Switched model, g0,1 and g2,3 are the 0/1 PWM signals.
 - For Sub-cycle average model, g0,1 and g2,3 can be either the 0/1
 PWM signals or the duty cycles between 0 and 1.
- The output V is the measured voltage across the DC bus.
- The output I is the measured output current.

- The connection port DC+ is the electrical port connected to the positive pole of the DC bus.
- The connection port DC- is the electrical port connected to the negative pole of the DC bus.
- The connection port N is the electrical port connected to the midpoint of the DC bus.
- The connection port A and B are the electrical ports connected to the AC output.



Parameters

- Modeling level selects the modeling level of the peripheral circuits.
- Transistor model type selects the model of the power transistors.
- Full-bridge module selects the type of PEH products to be simulated.
- DC Bus midpoint terminal visible shows or hides the port N.
- Initial DC voltage [V] defines the initial voltage across the DC bus when the simulation starts.



Probe signals

The following signals can be monitored by a Probe block in PLECS.

- Gate signals monitors the gate signals present at the input g0,1 and g2,3.
- DC Bus voltage true value [V] monitors the true value of the DC bus voltage in Volt.
- DC Bus voltage sensor output [V] monitors the physical output of the DC bus voltage sensor in Volt.
- Output current true value [A] monitors the true value of the output current in Amp.
- Output current sensor output [V] monitors the physical output of the output current sensor in Volt.

