PEN – NPC phase-leg

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The PEN block is a simulation model included in the Imperix Power library. It models the imperix NPC phase-leg PEN8018 in Simulink and PLECS simulation. For more information regarding how to get started with Imperix Power library, please read PN150.

This block also provides a thermal model for PEN8018. For more information regarding thermal simulation with the Imperix Power library, please read PN132.

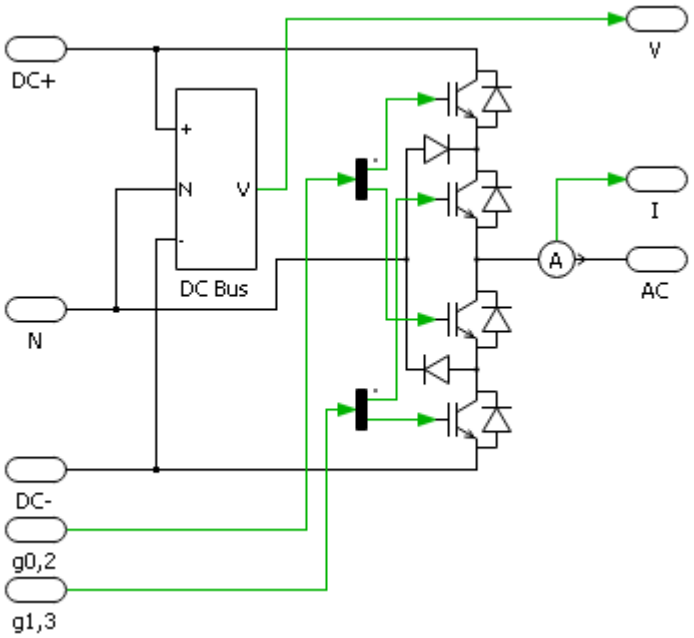
Imperix Power library is available starting from ACG SDK 2024.2. Moreover, thermal simulation is enabled from ACG SDK 2025.1 BETA. Simulink Simscape Electrical or

PLECS is also required. The Simulink version is only compatible with Specialized Power Systems. The supported versions are:
• Simulink R2016a or newer.
• Plexim PLECS 4.5 or newer.

Electrical modeling of PEN

The schematic of the electrical model of PEN is depicted on the right. It has two modeling levels:

- **(A) Simple**
- **(B) Detailed**

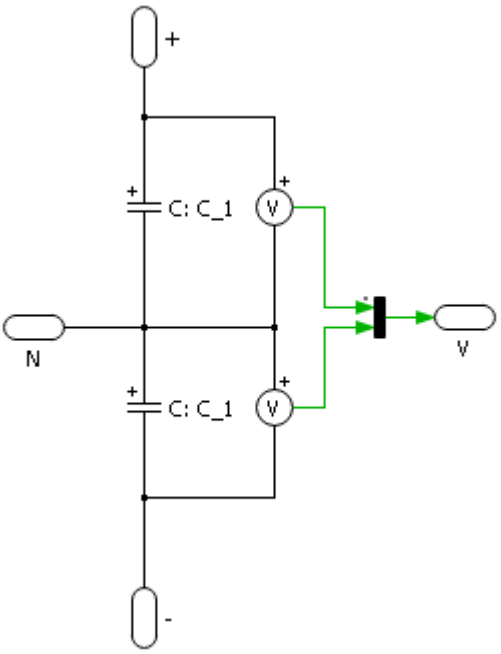


Schematic of PEN model

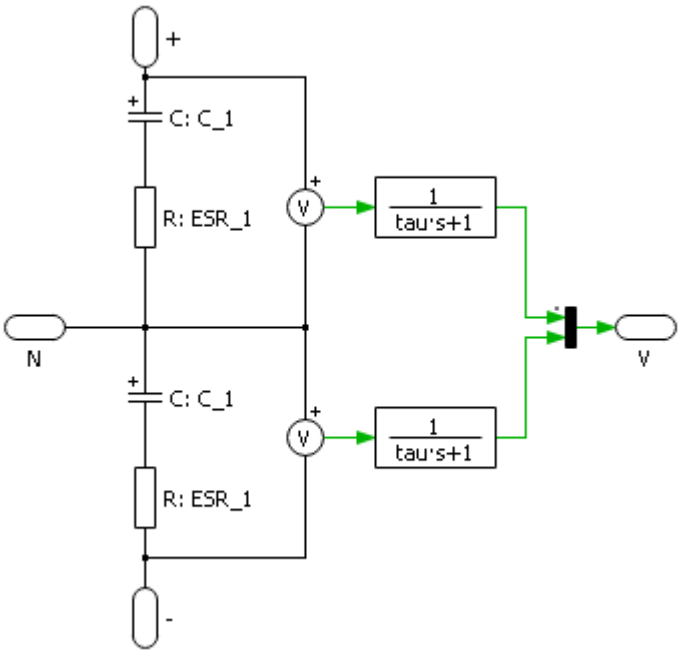
For more detailed model parameters and measurement results, please contact .

DC bus

The schematic of the equivalent DC bus is shown below.

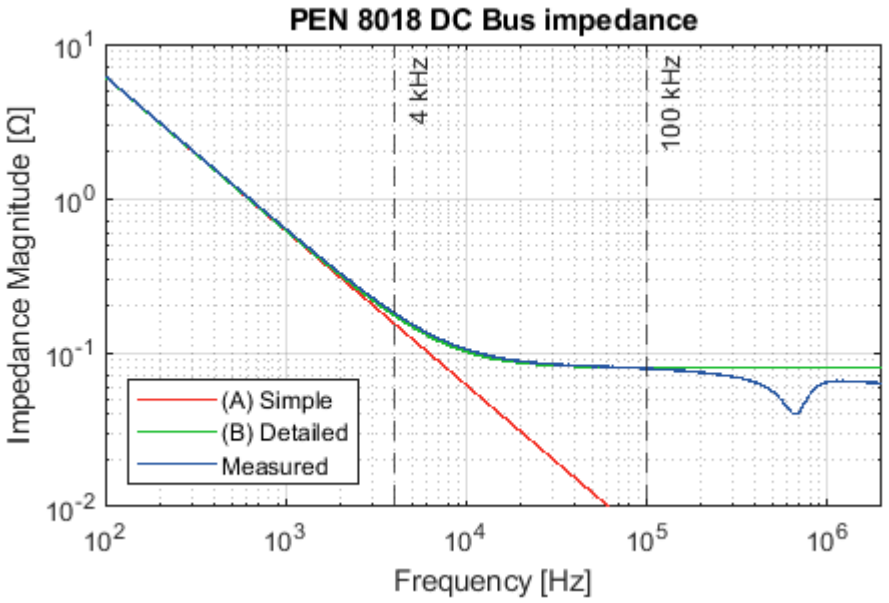


(A) Simple



(B) Detailed

The simulation model is relevant within a given frequency range. The frequency validity range is 0-4 kHz for the (A) Simple level and 0-100 kHz for the (B) Detailed level. In that range, the impedance and transfer function of the model are reasonably close to the modeled system, which can be seen along with the plots of the proposed models. The model parameters are also displayed below.

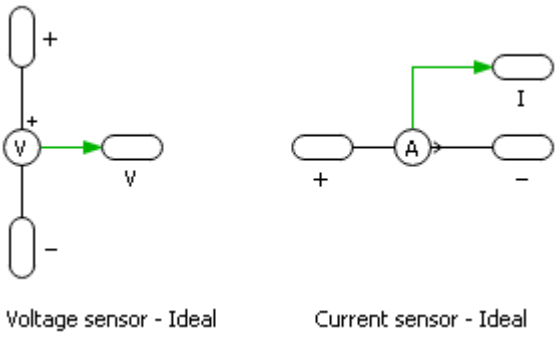


	C_1 [uF]	ESR_1 [mΩ]
(A)	258.5*2	0
(B)	258.5*2	80/2

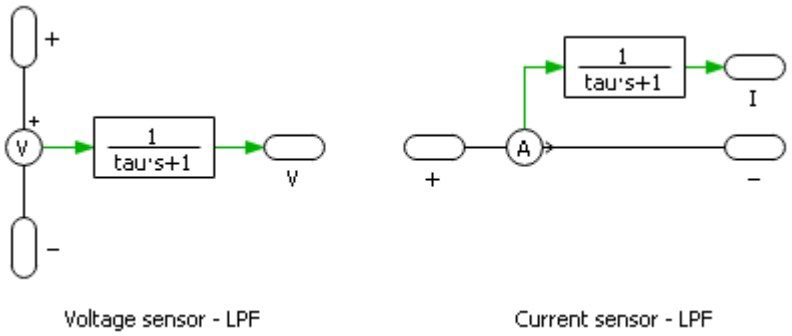
Model Parameters of PEN8018

Embedded sensors

A generic sensor can be approximately modeled by an ideal sensor in series with an optional first-order Low-Pass Filter (LPF). The relationship between sensor's bandwidth f_{BW} and the time constant τ of the LPF follows $\tau = \frac{1}{2\pi f_{BW}}$.



Ideal model



1st-order LPF model

A sensor is modeled as a first-order LPF only if its bandwidth lies within the frequency range of a given modeling level. Otherwise, it is modeled as an ideal sensor. The following table summarizes the information on all the sensors in the PEN.

Sensor	Bandwidth [kHz]	(A) Simple	(B) Detailed
PEN voltage sensor	25	Ideal	LPF
PEN current sensor	450	Ideal	Ideal

Modeling of the sensors in PEN

Power transistors

The PEN block offers two options for modeling the power transistors:

- **Switched** The transistors are modeled by individual power semiconductors. The control inputs are instantaneous logical gate signals.
- **Averaged** The transistors are modeled by controlled voltage and current sources. The control inputs are the relative on-times of the semiconductors with values between 0 and 1. The gate signals can be either instantaneous (using only values 0 and 1) or time-averaged.

Although the functionality is practically the same, these options are named differently in PLECS and Simulink Simscape to be consistent with their naming conventions.

In Simulink Simscape only the **Switched** model is available, which is named:

- **Switching devices**

In PLECS they are named:

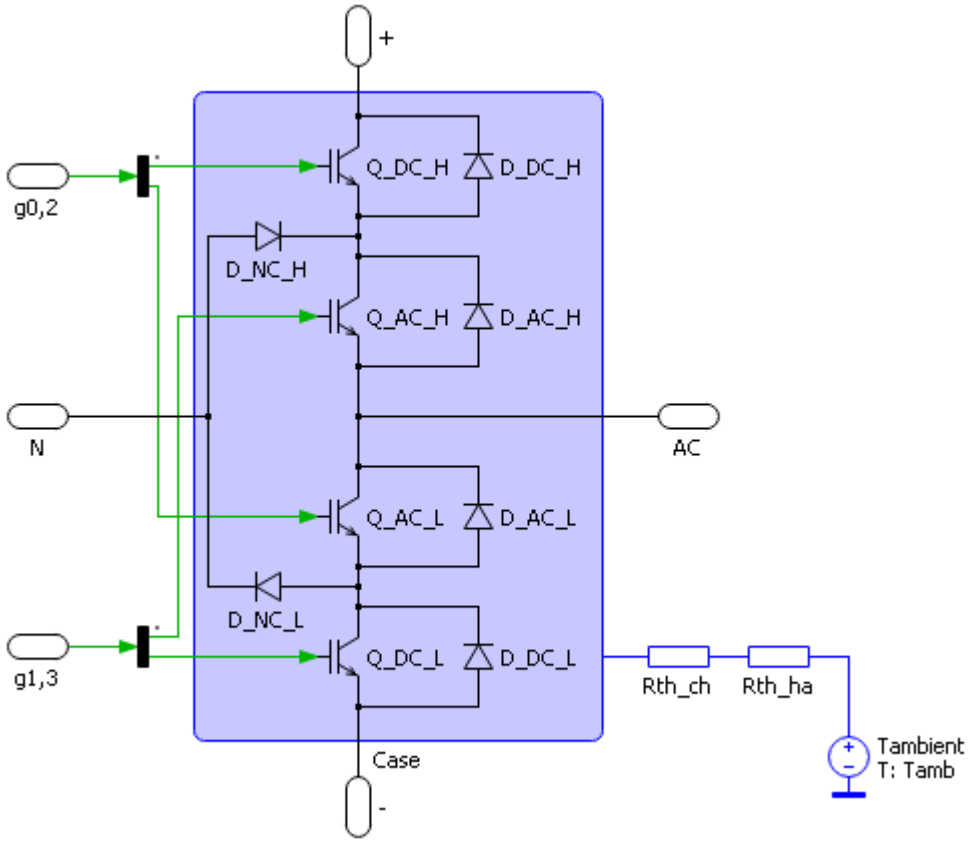
- **Switched**

- **Sub-cycle average**

Thermal modeling of PEN

The schematic of the thermal model of PEN8018 is depicted on the right.

It includes the loss model of the semiconductors and the thermal impedance network between the junction and the ambient temperature.



Schematic of PEB thermal model

Thermal impedance network

The thermal impedance model models only the thermal resistances, and all the thermal capacitances are either ignored or fixed at a small value to reduce the simulation time for the system to reach a thermal steady state. The model parameters are displayed below. Note that the thermal impedance between the junction and the case is included in the transistor's thermal description file and thus is not present in the schematic.

Thermal resistance	Value [K/W]
IGBT junction to case resistance	1.49

Diode junction to case resistance	1.819
Case to Heatsink resistance Rth_ch	1.91
Heatsink to ambient temperature resistance Rth_ha	0.21

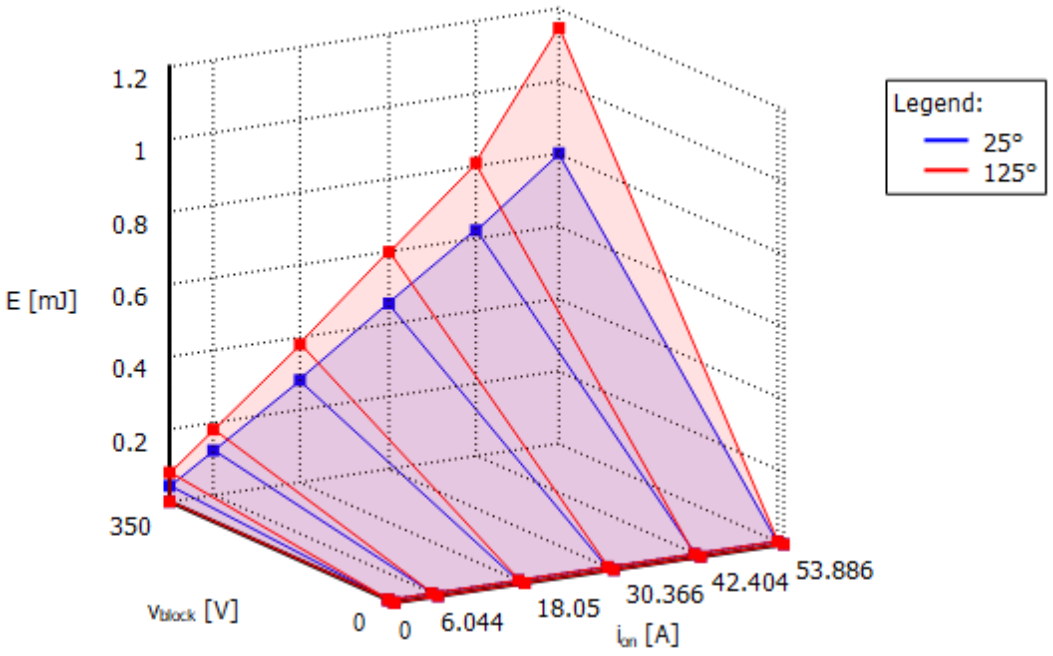
Thermal impedance model parameters of PEN8018

Semiconductor loss model

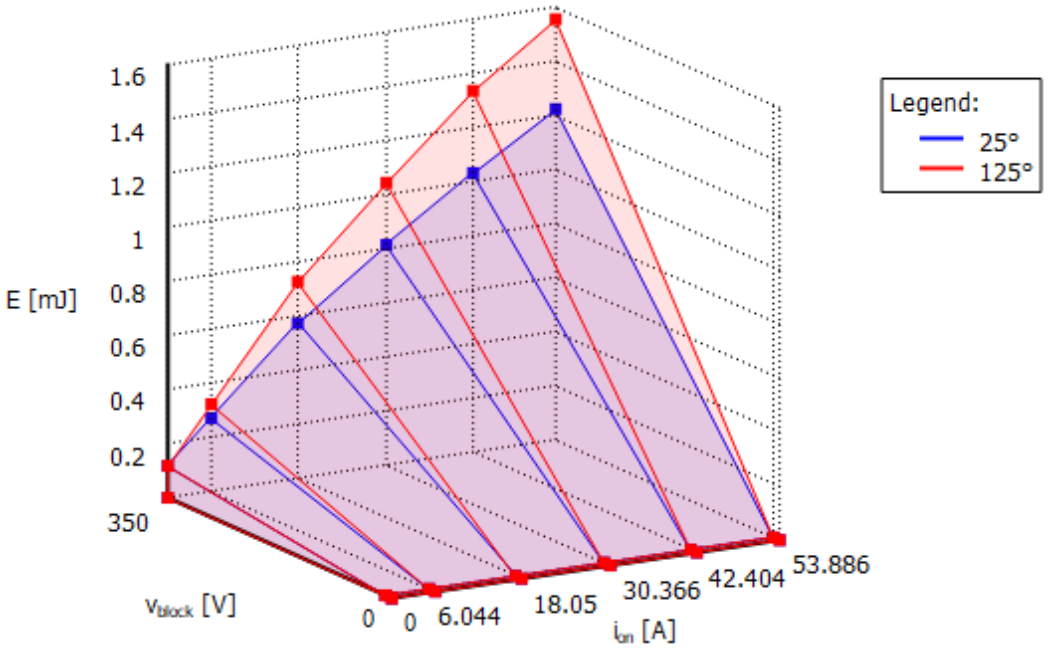
The semiconductor's turn-on loss E_{on}, turn-off loss E_{off}, and on-state drain-to-source voltage V_{on} are modeled by look-up-tables provided by manufacturers. The module's switching loss P_{sw} is calculated by periodic impulse averages of E_{on} and E_{off} over a chosen period, which is 1ms by default. The conduction loss P_{cond} is calculated by $P_{cond} = V_{on} \cdot I_{on}$. The detailed model implementation in Simulink and PLECS can be viewed in PN132, and the look-up-tables are provided below.

Look-up-tables of PEN8018

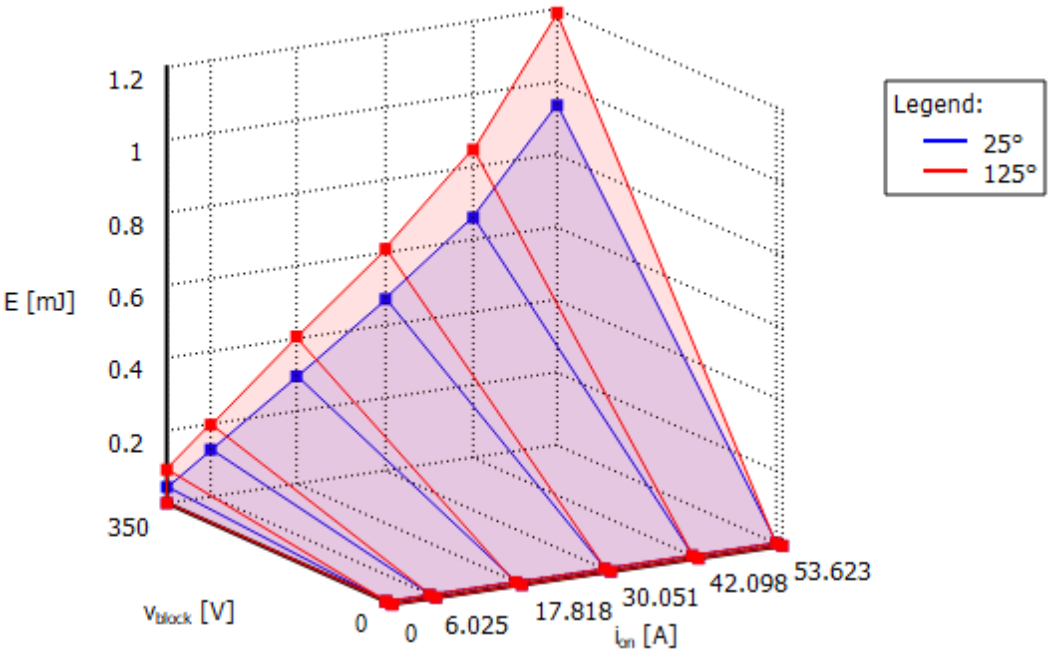
The look-up-tables of the Vincotech 10-FZ06NIA030SA-P924F33 used in PEN8018 are shown below.



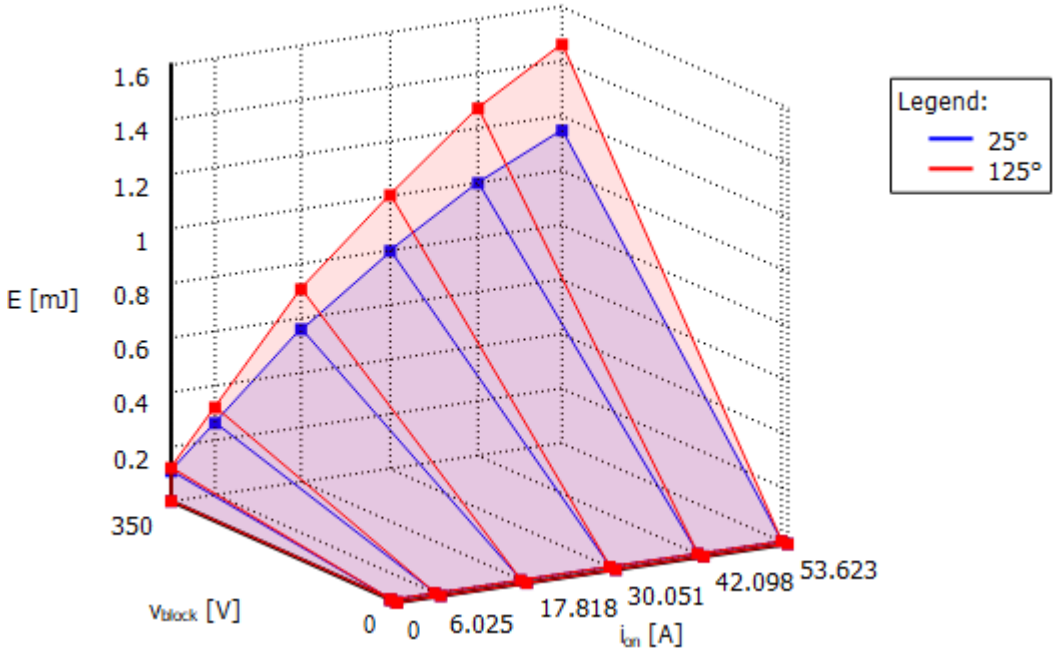
PEN8018 AC IGBT Eon



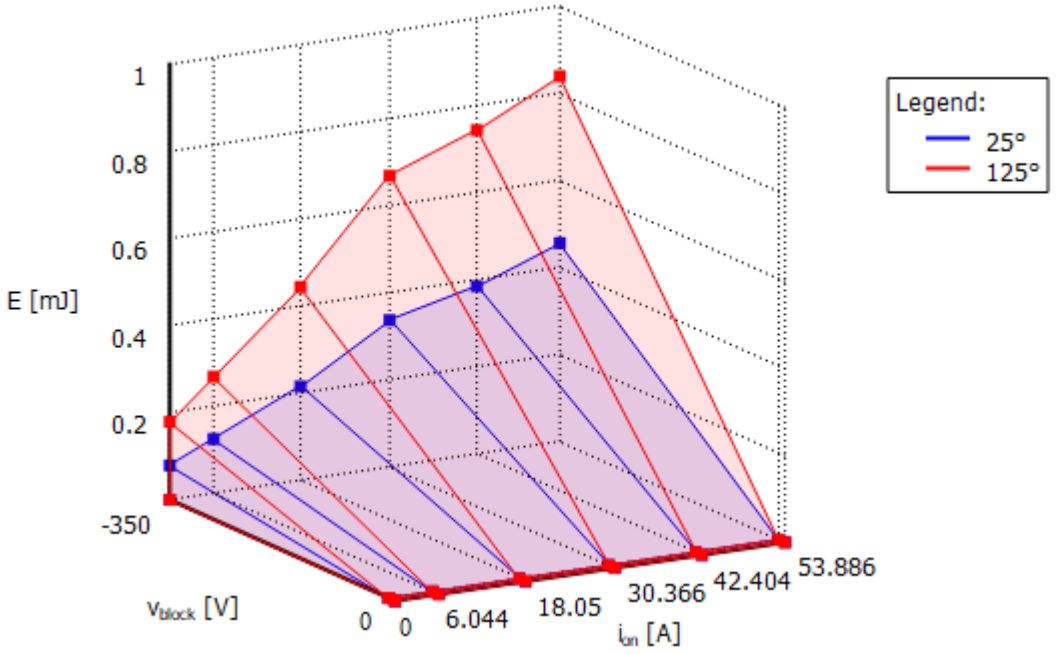
PEN8018 AC IGBT Eoff



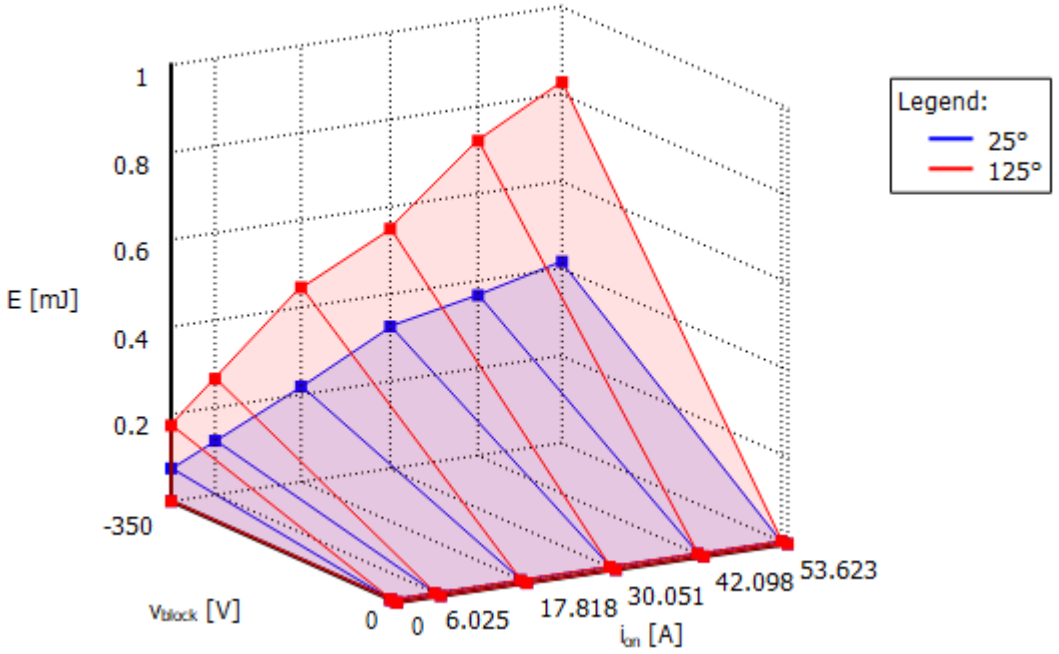
PEN8018 DC IGBT Eon



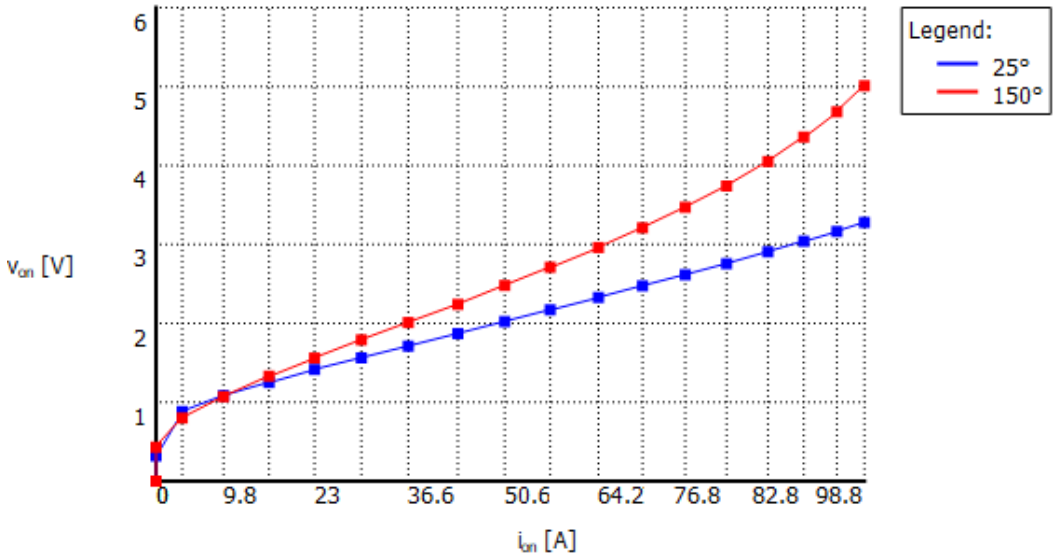
PEN8018 DC IGBT Eoff



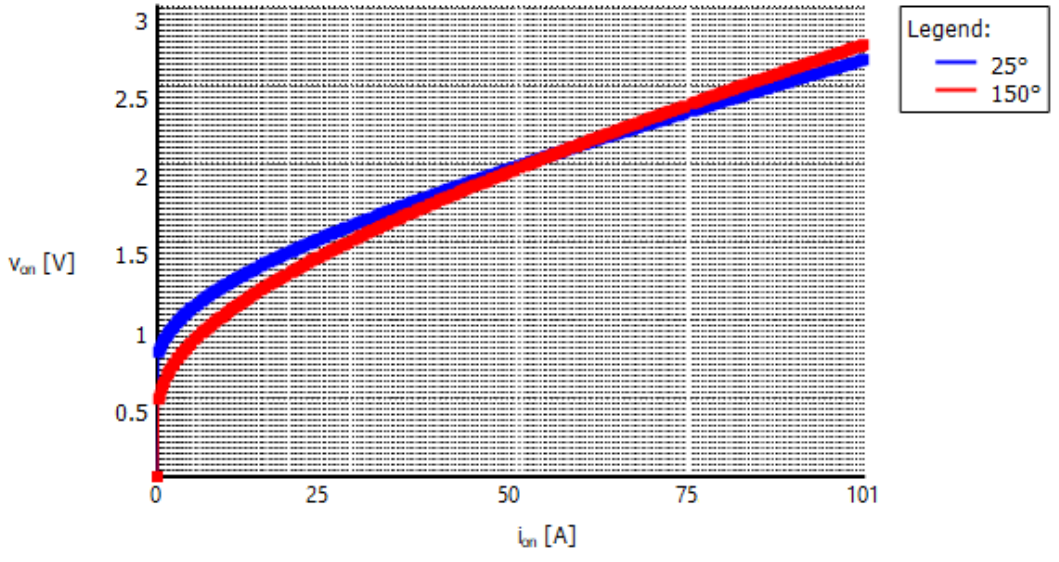
PEN8018 DC Diode Eoff



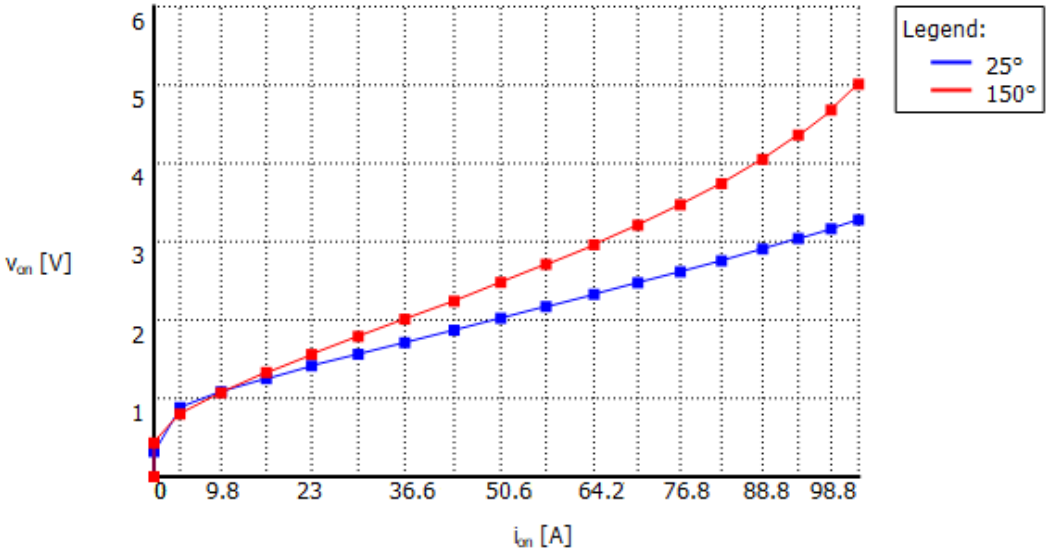
PEN8018 NC Diode Eoff



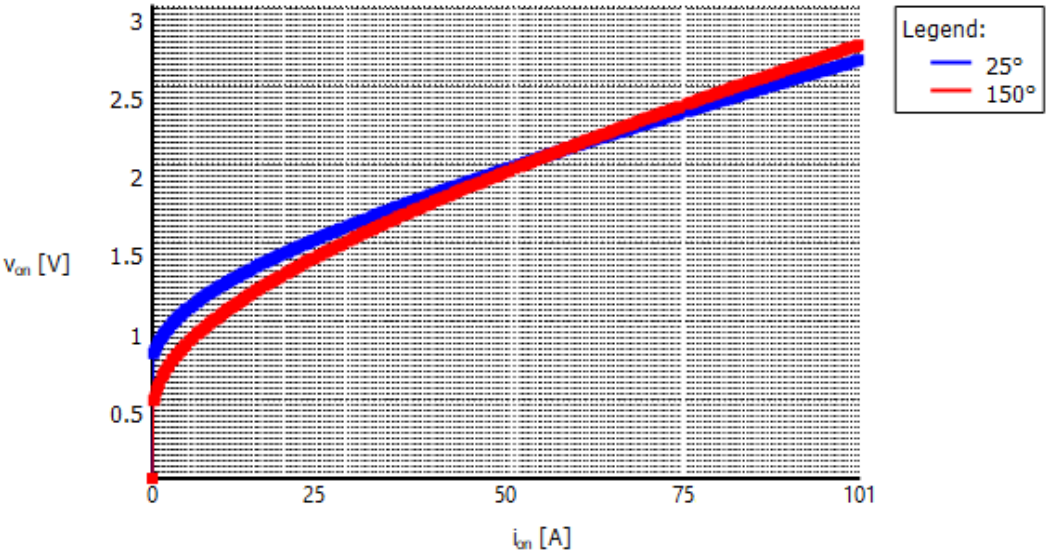
PEN8018 AC IGBT Von



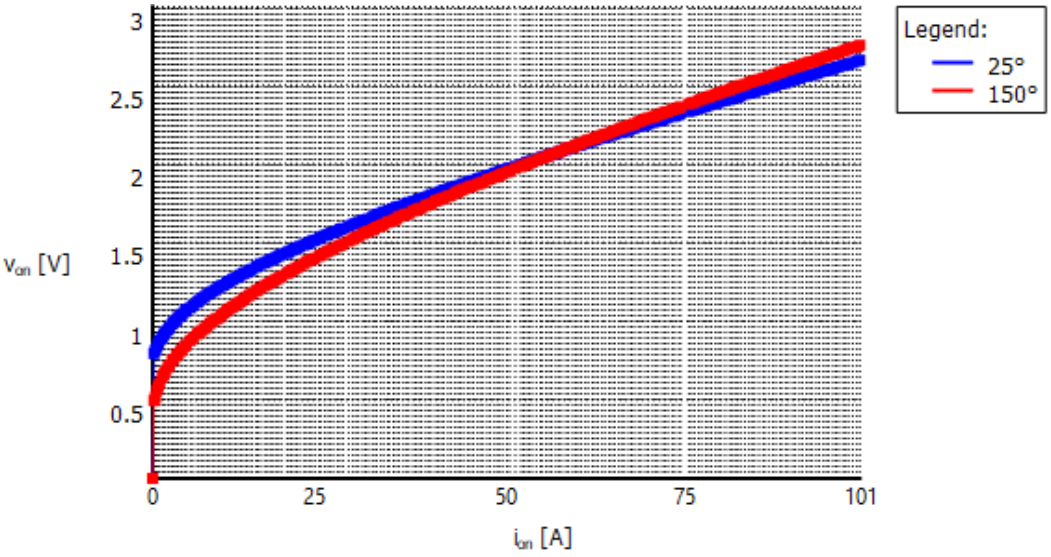
PEN8018 AC Diode Von



PEN8018 DC IGBT Von



PEN8018 DC Diode Von

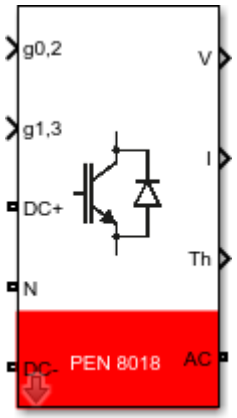


PEN8018 NC Diode Von

Simulink PEN block

Port specification

- The input `g0,2` and `g1,3` are the gate signals. There are 4 signals in total, and the order is shown in the schematic.
  - For `Switching devices (switched)` model, `g0,2` and `g1,3` are the 0/1 PWM signals.
  - For `Switching Function (averaged)` model, `g0,2` and `g1,3` can be either the 0/1 PWM signal or the duty cycle between 0 and 1.
- The output `V` is the measured voltages across each half of the DC bus.
- The output `I` is the measured output current.
- The output `Th` is the thermal simulation results. This port is only visible when thermal simulation is enabled.
- The connection port `DC+` is the electrical port connected to the positive pole of the DC bus.
- The connection port `DC-` is the electrical port connected to the negative pole of the DC bus.
- The connection port `N` is the electrical port connected to the midpoint of the DC bus.
- The connection port `AC` is the electrical port connected to the AC output.

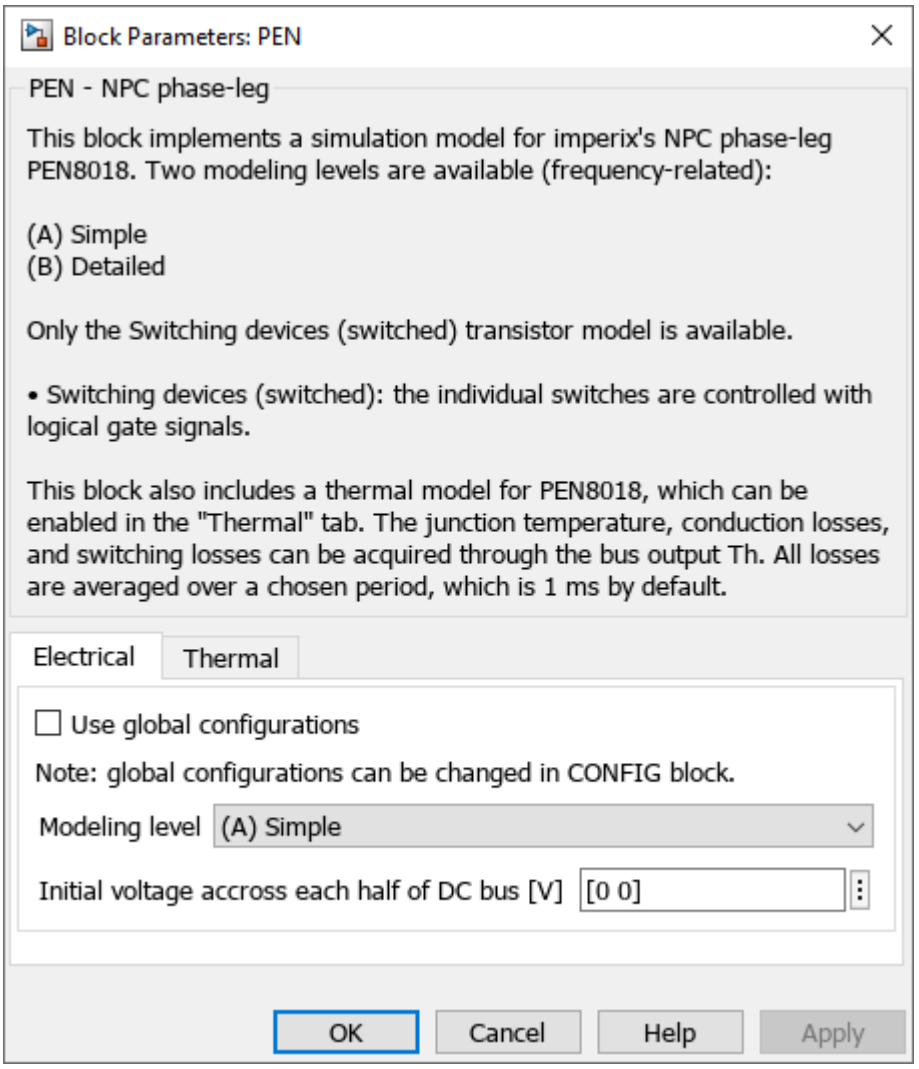


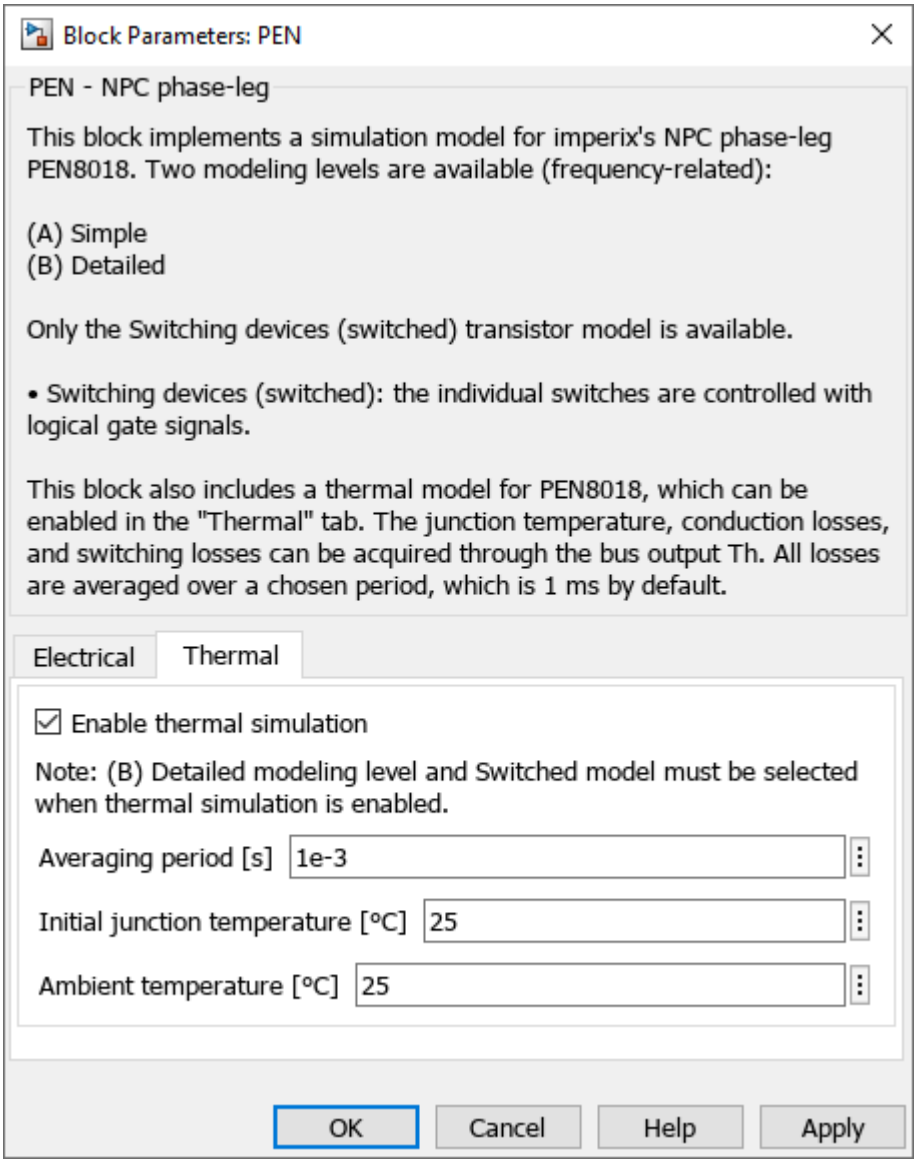
Electrical parameters

- `Use global configurations` is ticked when the block receives global configurations from the `Config` block.
- `Modeling level` selects the modeling level of the peripheral circuits.
- `Initial voltage across each half of DC Bus [V]` is a 2×1 array that defines the initial voltage across each half of the DC bus when the simulation starts.

Thermal parameters

- `Enable thermal simulation` is ticked when the thermal simulation is enabled.
- `Averaging period [s]` defines the averaging period for calculating switching loss.
- `Initial junction temperature [°C]` defines the initial junction temperature when the simulation starts.
- `Ambient temperature [°C]` defines the ambient temperature throughout the simulation.



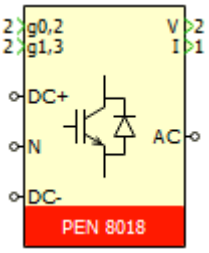


PLECS PEN block

Port specification

- The input `g0,2` and `g1,3` are the gate signals. There are 4 signals in total, and the order is shown in the schematic.
  - For `Switched` model, `g0,2` and `g1,3` are the 0/1 PWM signals.
  - For `Sub-cycle average` model, `g0,2` and `g1,3` can be either the 0/1 PWM signals or the duty cycles between 0 and 1.
- The output `V` is the measured voltages across each half of the DC bus.
- The output `I` is the measured output current.
- The connection port `DC+` is the electrical port connected to the positive pole of the DC bus.
- The connection port `DC-` is the electrical port connected to the negative pole of the DC bus.

- The connection port `N` is the electrical port connected to the midpoint of the DC bus.
- The connection port `AC` is the electrical port connected to the AC output.

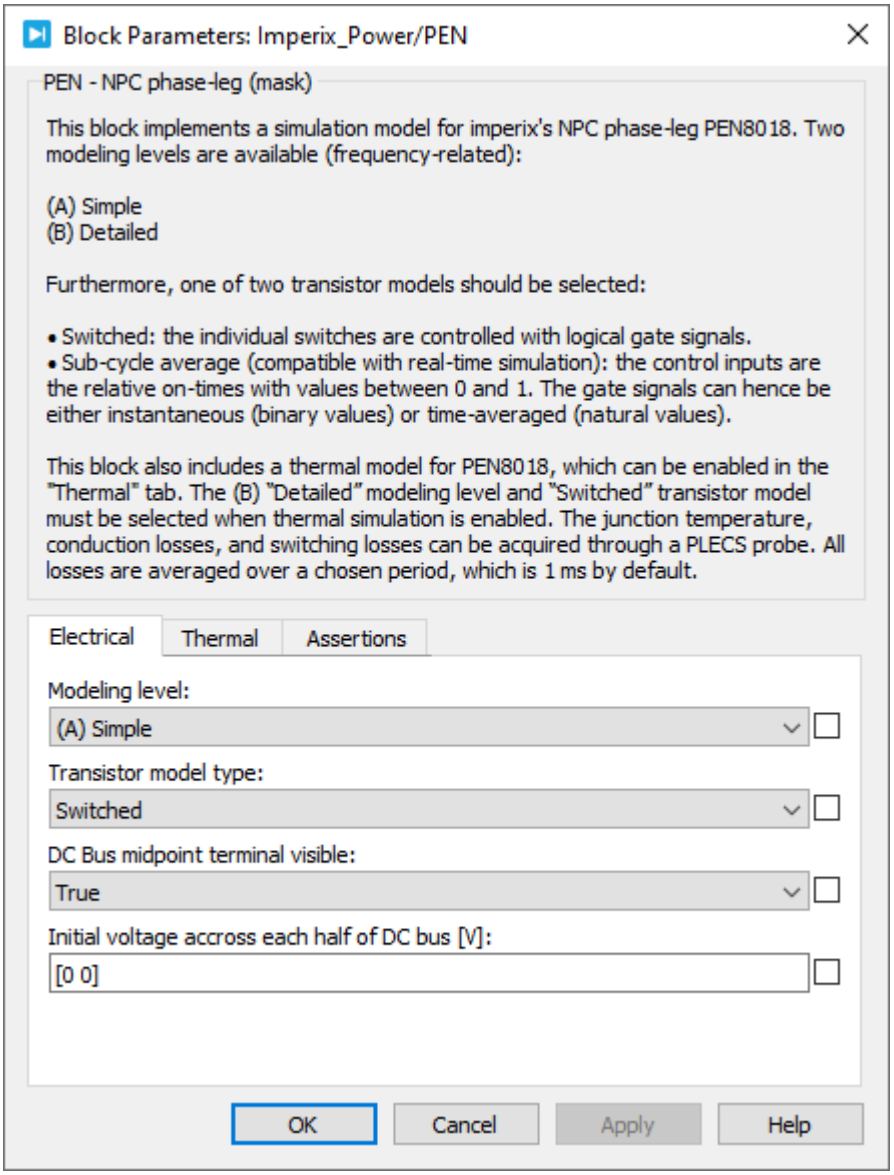


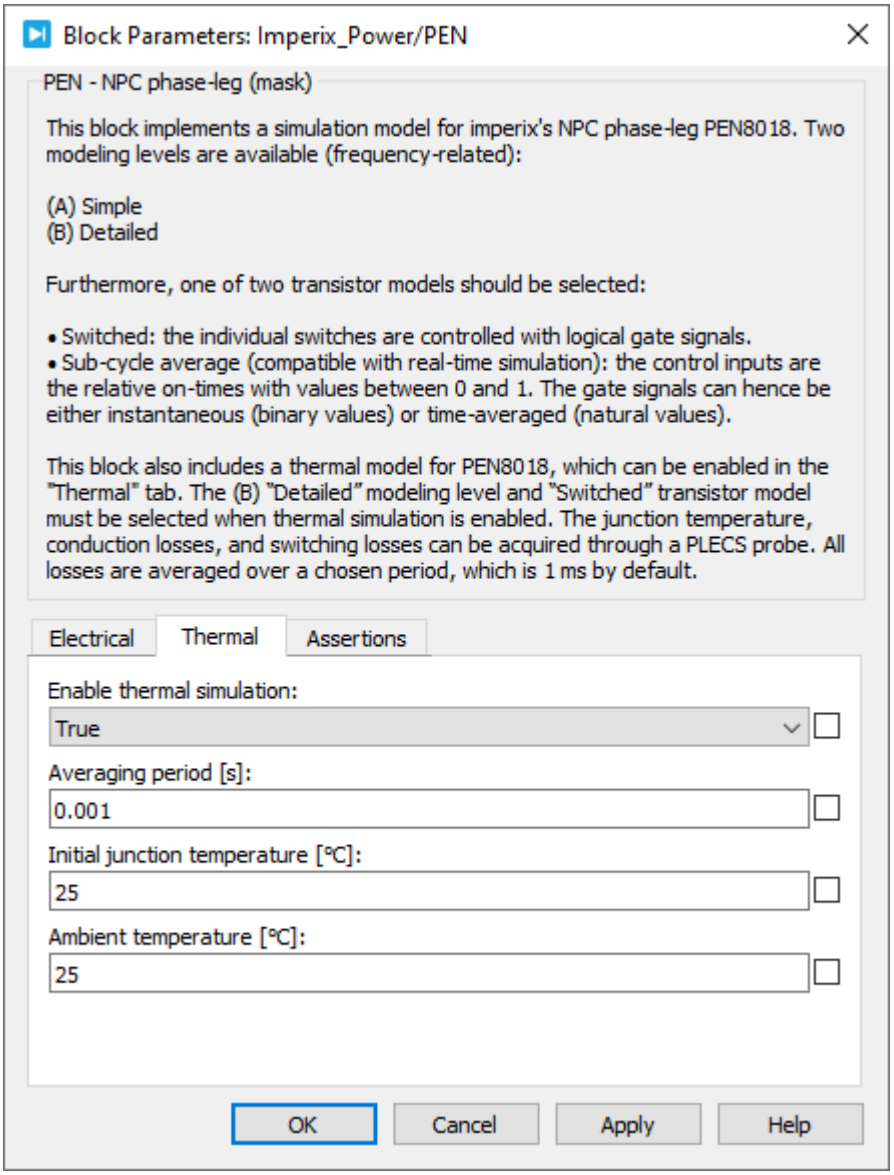
Electrical parameters

- `Modeling level` selects the modeling level of the peripheral circuits.
- `Transistor model type` selects the model of the power transistors.
- `DC Bus midpoint terminal visible` shows or hides the port `N`.
- `Initial voltage across each half of DC Bus [V]` is a 2×1 array that defines the initial voltage across each half of the DC bus when the simulation starts.

Thermal parameters

- `Enable thermal simulation` is ticked when the thermal simulation is enabled.
- `Averaging period [s]` defines the averaging period for calculating switching loss.
- `Initial junction temperature [°C]` defines the initial junction temperature when the simulation starts.
- `Ambient temperature [°C]` defines the ambient temperature throughout the simulation.


Block Parameters: Imperix_Power/PEN
PEN - NPC phase-leg (mask)
This block implements a simulation model for imperix's NPC phase-leg PEN8018. Two modeling levels are available (frequency-related):
(A) Simple
(B) Detailed
Furthermore, one of two transistor models should be selected:
• Switched: the individual switches are controlled with logical gate signals.
• Sub-cycle average (compatible with real-time simulation): the control inputs are the relative on-times with values between 0 and 1. The gate signals can hence be either instantaneous (binary values) or time-averaged (natural values).
This block also includes a thermal model for PEN8018, which can be enabled in the "Thermal" tab. The (B) "Detailed" modeling level and "Switched" transistor model must be selected when thermal simulation is enabled. The junction temperature, conduction losses, and switching losses can be acquired through a PLECS probe. All losses are averaged over a chosen period, which is 1 ms by default.
Electrical
Thermal
Assertions
Modeling level:
(A) Simple
Transistor model type:
Switched
DC Bus midpoint terminal visible:
True
Initial voltage accross each half of DC bus [V]:
[0 0]
OK
Cancel
Apply
Help



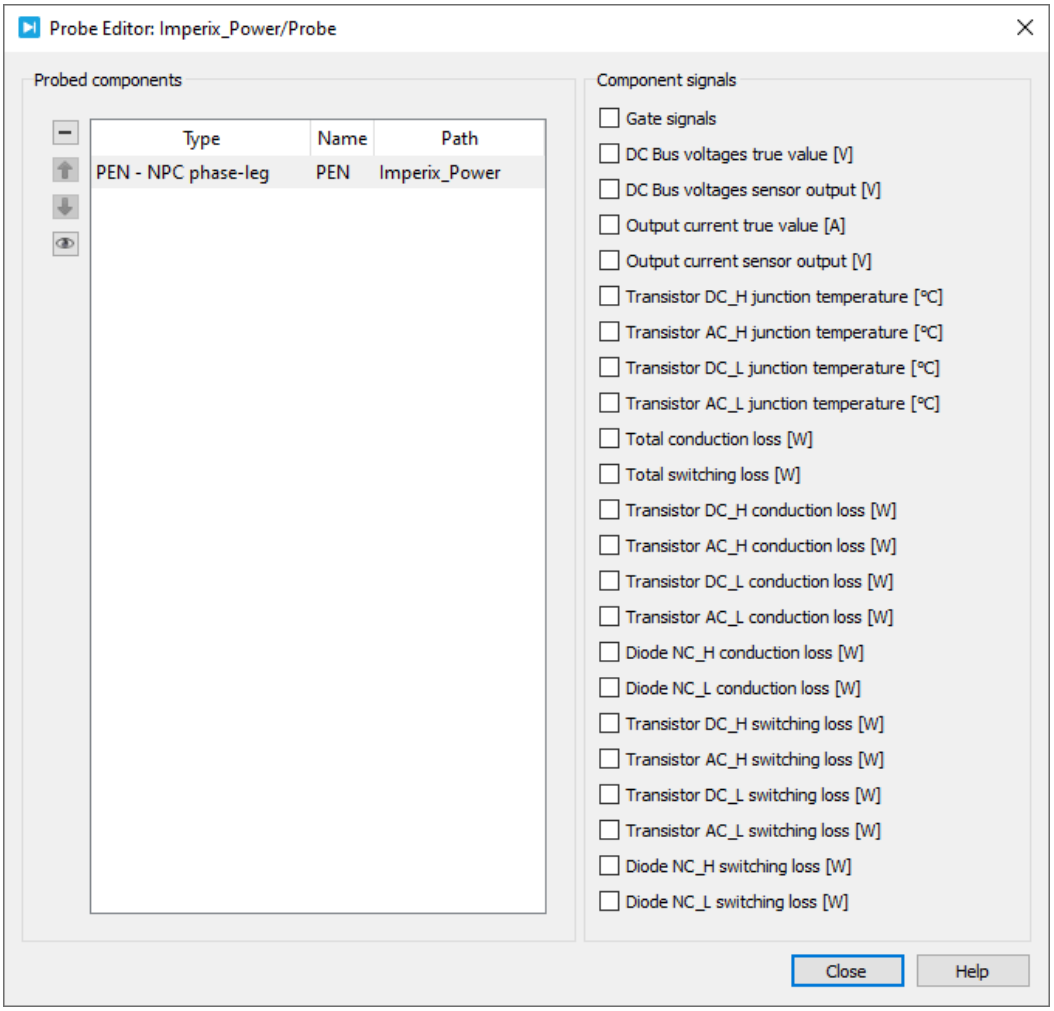
Probe signals

The following signals can be monitored by a Probe block in PLECS.

- `Gate signals` monitors the gate signals present at the input g.
- `DC Bus voltages true value [V]` monitors the true value of the DC bus voltages in Volt.
- `DC Bus voltages sensor output [V]` monitors the physical output of the DC bus voltage sensors in Volt.
- `Output current true value [A]` monitors the true value of the output current in Amp.
- `Output current sensor output [V]` monitors the physical output of the output current sensor in Volt.

The following signals contain thermal simulation results that can be monitored when thermal simulation is enabled.

- `Transistor DC_H junction temperature [°C]` monitors the junction temperature of transistor DC_H in °C.
- `Transistor AC_H junction temperature [°C]` monitors the junction temperature of transistor AC_H in °C.
- `Transistor DC_L junction temperature [°C]` monitors the junction temperature of transistor DC_L in °C.
- `Transistor AC_L junction temperature [°C]` monitors the junction temperature of transistor AC_L in °C.
- `Total conduction loss [W]` monitors the module's total conduction loss in Watt.
- `Total switching loss [W]` monitors the module's total switching loss in Watt.
- `Transistor DC_H conduction loss [W]` monitors the conduction loss of transistor DC_H in Watt.
- `Transistor AC_H conduction loss [W]` monitors the conduction loss of transistor AC_H in Watt.
- `Transistor DC_L conduction loss [W]` monitors the conduction loss of transistor DC_L in Watt.
- `Transistor AC_L conduction loss [W]` monitors the conduction loss of transistor AC_L in Watt.
- `Diode NC_H conduction loss [W]` monitors the conduction loss of diode NC_H in Watt.
- `Diode NC_L conduction loss [W]` monitors the conduction loss of diode NC_L in Watt.
- `Transistor DC_H switching loss [W]` monitors the switching loss of transistor DC_H in Watt.
- `Transistor AC_H switching loss [W]` monitors the switching loss of transistor AC_H in Watt.
- `Transistor DC_L switching loss [W]` monitors the switching loss of transistor DC_L in Watt.
- `Transistor AC_L switching loss [W]` monitors the switching loss of transistor AC_L in Watt.
- `Diode NC_H switching loss [W]` monitors the switching loss of diode NC_H in Watt.
- `Diode NC_L switching loss [W]` monitors the switching loss of diode NC_L in Watt.


Probe Editor: Imperix_Power/Probe
Probed components
Type
Name
Path
PEN - NPC phase-leg
PEN
Imperix_Power
Component signals
Gate signals
DC Bus voltages true value [V]
DC Bus voltages sensor output [V]
Output current true value [A]
Output current sensor output [V]
Transistor DC_H junction temperature [°C]
Transistor AC_H junction temperature [°C]
Transistor DC_L junction temperature [°C]
Transistor AC_L junction temperature [°C]
Total conduction loss [W]
Total switching loss [W]
Transistor DC_H conduction loss [W]
Transistor AC_H conduction loss [W]
Transistor DC_L conduction loss [W]
Transistor AC_L conduction loss [W]
Diode NC_H conduction loss [W]
Diode NC_L conduction loss [W]
Transistor DC_H switching loss [W]
Transistor AC_H switching loss [W]
Transistor DC_L switching loss [W]
Transistor AC_L switching loss [W]
Diode NC_H switching loss [W]
Diode NC_L switching loss [W]
Close
Help