AXI4-Stream IPs from Xilinx

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This page presents some useful Xilinx IP cores for Vivado. These IPs use the widely used AXI4-Stream protocol to easily exchange data with other Xilinx IPs or with user-made algorithms developed using High-Level Synthesis (HLS) design tools such as Model Composer or Vitis HLS.

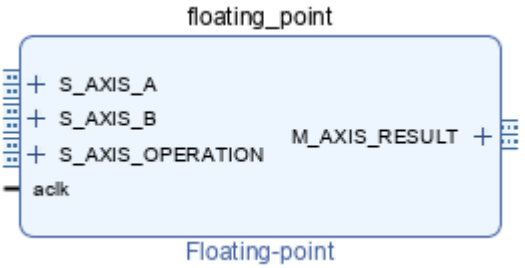
For more detailed information on the AXI4-Stream interconnect protocol, please refer to AMBA®4 AXI4-Stream Protocol Specification.

To find all FPGA-related notes, you can visit FPGA development homepage.

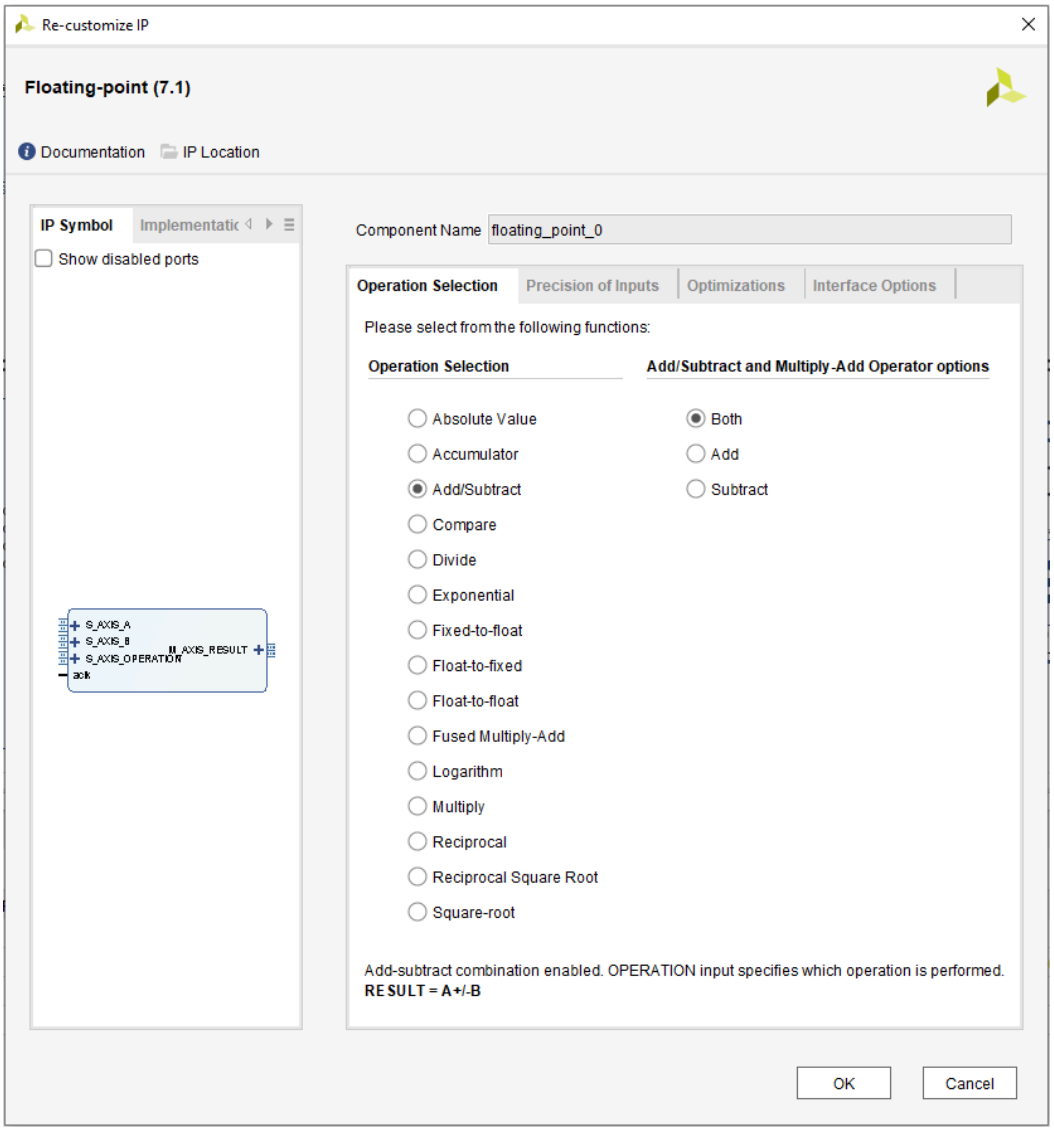
Floating-point IP

Xilinx Floating-point IPs can be used to deal with most floating-point computations. The operation, precision, optimization, latency can be customized.

In Vivado, open the block design, right-click somewhere, and chose **Add IP…** Search for **Floating-point** and drag it into the diagram.



Double-click on the block and configure the block in the pop-up window.

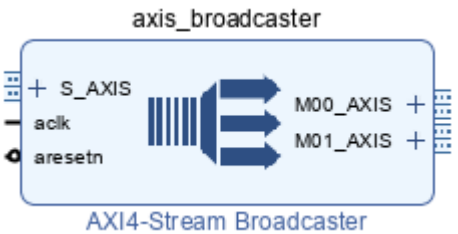


For more details please refer to [Floating-Point Operator v7.1 LogiCORE IP Product Guide (xilinx.com)](xilinx.com).

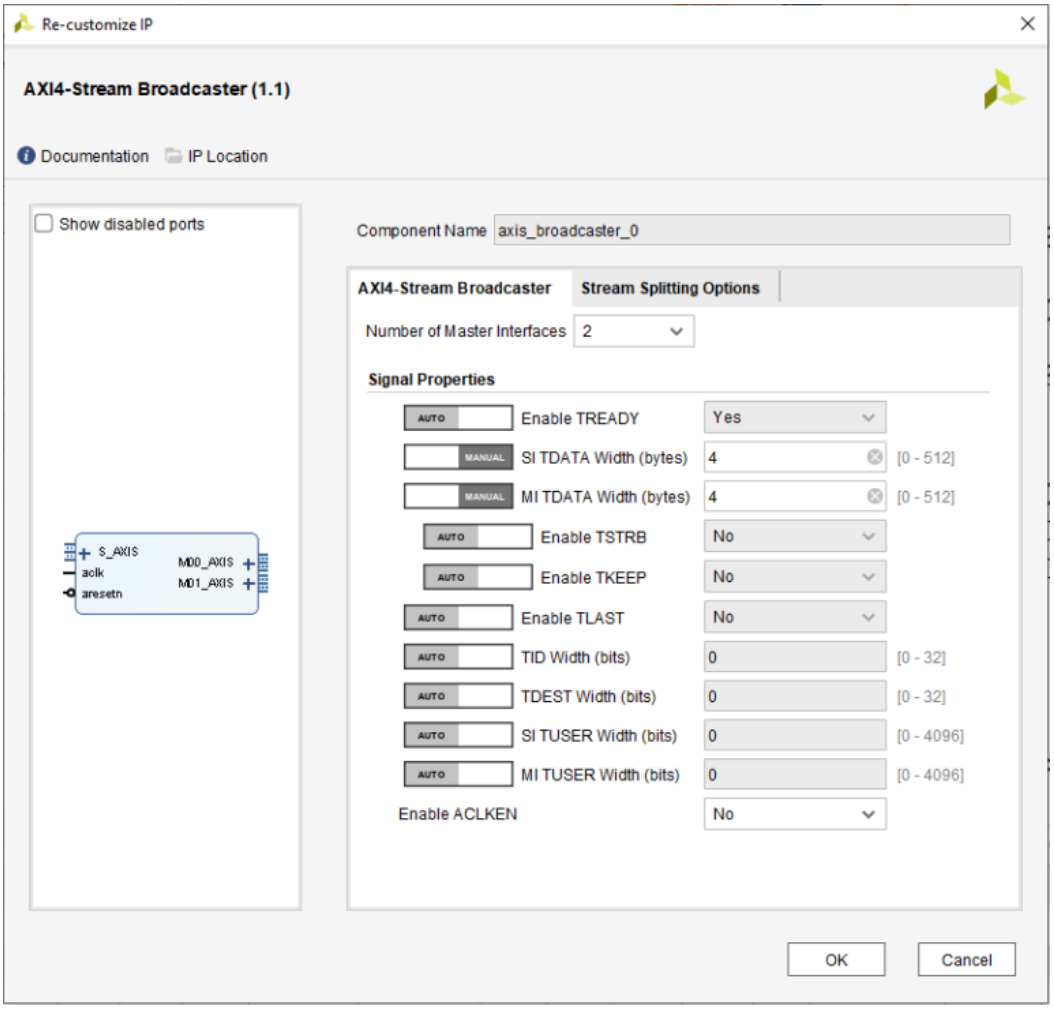
AXI4-Stream Broadcaster

In some cases, it can be useful to send one data to multiple slaves, or copy one data and send it to the CPU for debugging. For that purpose, the AXI4-Stream Broadcaster can be used.

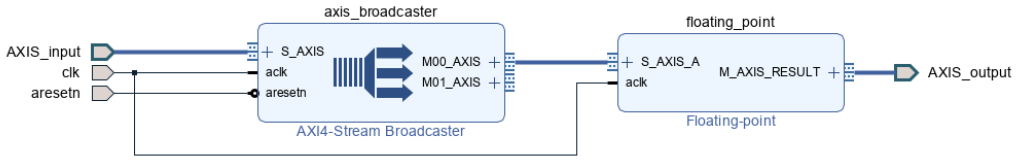
In Vivado, open the block design, right-click somewhere and chose **Add IP...** Search for **AXI4-Stream Broadcaster** and drag it into the diagram.



Double-click on the block and configure the block in the pop-up window. Usually, users only have to change the number of master interfaces and the SI/MI data width.



WARNING 1: Note that users should not leave the output ports floating or not connected to a AXI4-Stream slave. Since the AXI4-Stream Broadcaster IP doesn't provide a default *tready* signal, a floating output port will block the dataflow. A relevant discussion about the problem caused by floating *tready* is in [Solved: axis broadcaster – Community Forums (xilinx.com)]



The dataflow is blocked at M01_AXIS because no *tready* signal is received

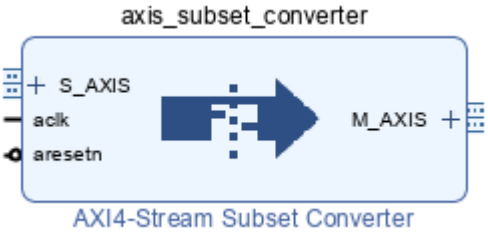
WARNING 2: There is a known bug of AXI4-Stream Broadcaster that the width of all the *tdata/tready/tvalid/…* signals looks "bigger" than normal. For example if one broadcasts a 4 Byte signal to 2 slaves, he will see a 8-Byte *tdata* in the output port, and this *tdata* cannot be overridden. This is only a display bug and users should only

refer to the real data width in the configuration window. A relevant discussion about the problem is in [Solved: using axi broadcaster – Community Forums (xilinx.com)](#).

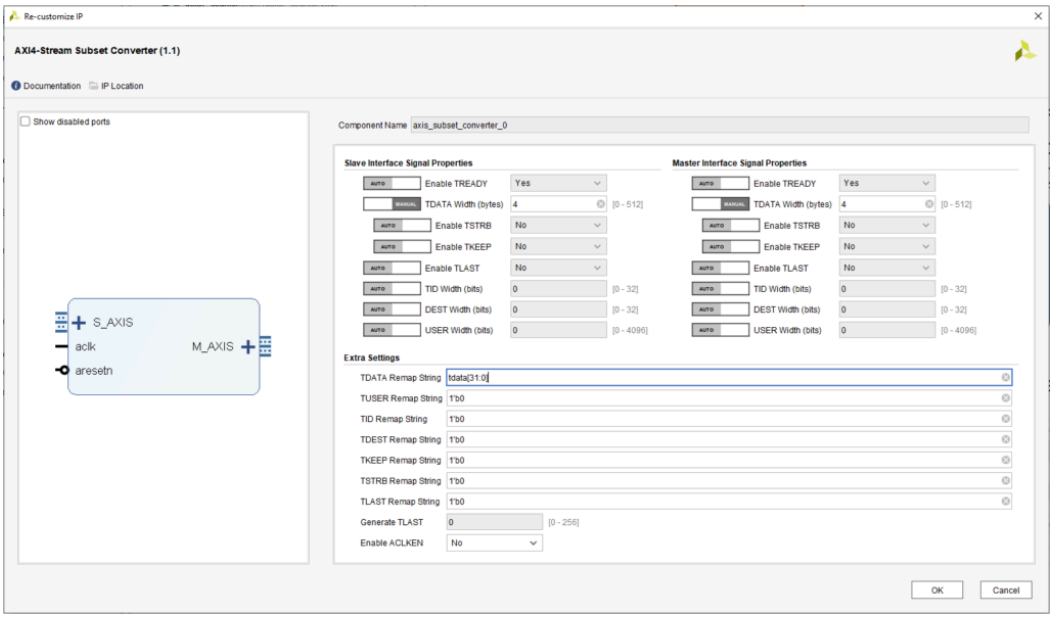
AXI4-Stream Subset Converter

This IP is used to extract a subset from an AXI4-Stream signal.

In Vivado, open the block design, right-click somewhere and chose **Add IP…** Search for **AXI4-Stream Subset Converter** and drag it into the diagram.



Double-click on the block and configure the block in the pop-up window. Usually, users only have to change the SI/MI data width.



For more details of AXI4-Stream Protocol Broadcaster and Subset Converter, please refer to [AXI4-Stream Infrastructure IP Suite v3.0 LogiCORE IP Product Guide (xilinx.com)](#).

Back to [FPGA development homepage](#)