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Control of a Five-Level NPC grid-tied inverter using a BoomBox control platform

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Introduction

The studied converter topology is shown in Figure 1. It consists of a conventional 5-level inverter connected to four equal and stabilized superposed voltage sources. At the converter output, a basic LC-type low-pass filter allows to reduce the switching harmonics present on the load current.

The purpose of this tutorial is to describe how multilevel modulation patterns can be implemented on the BoomBox control platform [4, 5]. The present document is an excerpt from a student semester conducted during summer 2015 at EPFL-LEI under supervision of Prof. A. Rufer. The overall results of the study have been further presented in [1, 2].

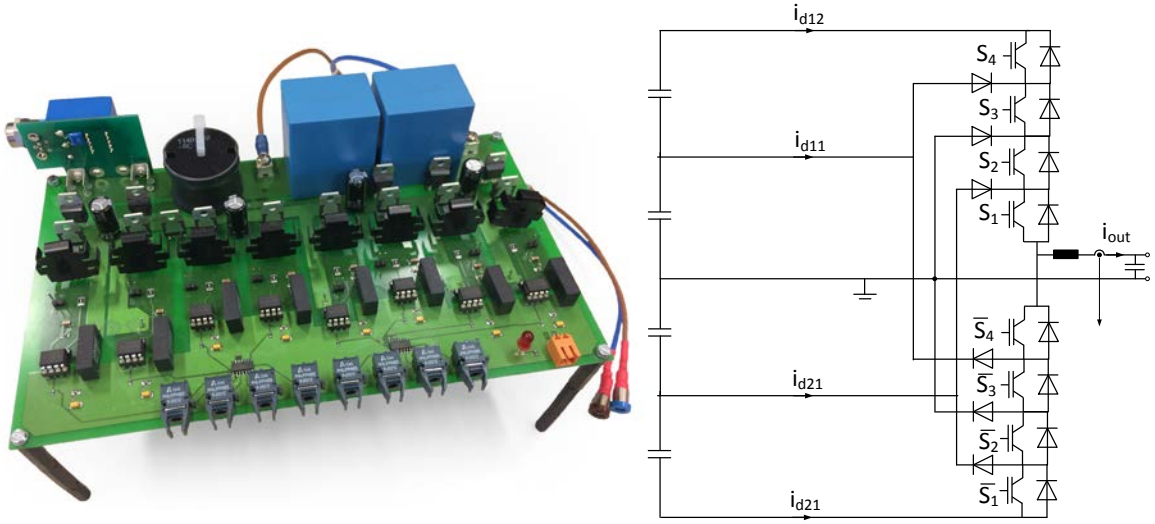

Figure 1: Photograph and schematic of the studied 5L-NPC converter topology.

Pulse-width modulation

Several types of multilevel pulse-width modulation are described in the literature. As presented in [3], these multiple types of modulation can generally be classified into three main categories of approaches, illustrated in Figure 2:

- PD, phase disposition
- POD, phase opposition disposition
- APOD, alternate phase opposition disposition

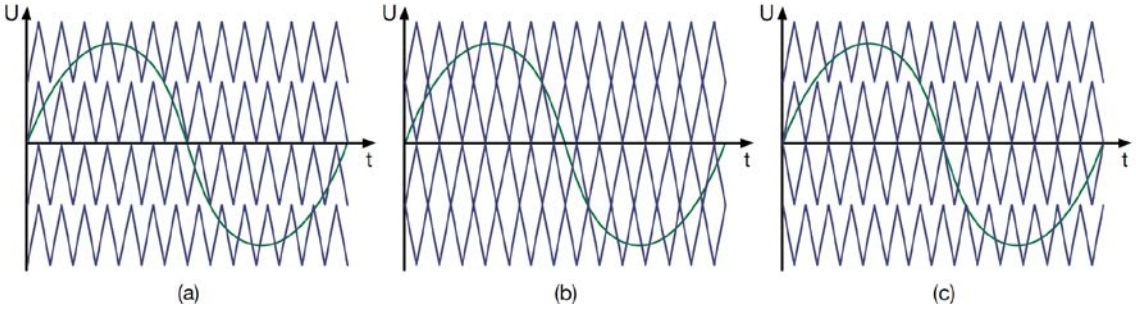

Figure 2: 5-level modulation approaches. (a) PD, (b) APOD, (c) POD.

For the purposes of this work, the phase disposition (PD) strategy is arbitrarily chosen. Nevertheless, the two other modulation strategies are also given in the code example so as to illustrate how these approaches could be implemented in the BoomBox as well.
Consequently, the configuration of the BoomBox control platform is done as follows:

1. Configuration of the main time base :

```
// Set a 20 kHz switching frequency on FREQGEN0:
SetFreqGenPeriod(FREQGEN0, (int)(SWITCHING_PERIOD/FPGA_CLK_PERIOD));
```

2. Configuration of the PWM channels:

```
// Channels #0-3 are mapped to FREQGEN0 with a triangular carrier:
ConfigPWMChannel(0, FREQGEN0, TRIANGLE, (int)(DEADTIME/FPGA_CLK_PERIOD));
ConfigPWMChannel(1, FREQGEN0, TRIANGLE, (int)(DEADTIME/FPGA_CLK_PERIOD));
ConfigPWMChannel(2, FREQGEN0, TRIANGLE, (int)(DEADTIME/FPGA_CLK_PERIOD));
ConfigPWMChannel(3, FREQGEN0, TRIANGLE, (int)(DEADTIME/FPGA_CLK_PERIOD));
```

3. Immediate activation of all PWMs:

```
// Channel #0-3 are immediately activated at startup:
ActivatePWMChannel(0);
ActivatePWMChannel(1);
ActivatePWMChannel(2);
ActivatePWMChannel(3);
```

Subsequently, in the main interrupt UserInterrupt1(), the following code must be placed:

4. Generation of a sinusoidal waveform of amplitude 0.7 and of frequency 50Hz:

```
// Generate a sinusoidal reference at 50Hz:
Uref = 0.7*sin(2*PI*OUTPUT_FREQUENCY*SWITCHING_PERIOD*time_sin);
time_sin++;
if(time_sin > ((SWITCHING_FREQUENCY/OUTPUT_FREQUENCY)-1)) {time_sin = 0;}
```

5. Generation of the duty cycles. The following code is equivalent to an equal distribution of the carriers in the interval [-1;1]:

```
// Compute the PWM duty-cycles:
Duty_A = (Uref-0.5)*2.0;
Duty_B = (Uref)*2.0;
Duty_C = (Uref+0.5)*2.0;
Duty_D = (Uref+1.0)*2.0;
```

6. Re-configuration of the PWMs :

```
// Apply the duty cycles:
SetPWMDutyCycle(0, Duty_A);
SetPWMDutyCycle(1, Duty_B);
SetPWMDutyCycle(2, Duty_C);
SetPWMDutyCycle(3, Duty_D);
```

7. Finally, update of all modulators:

```
UpdatePWMData();
```

Experimental results

The generated PWM gating signals correspond to the desired pattern, as shown by Figure 3:

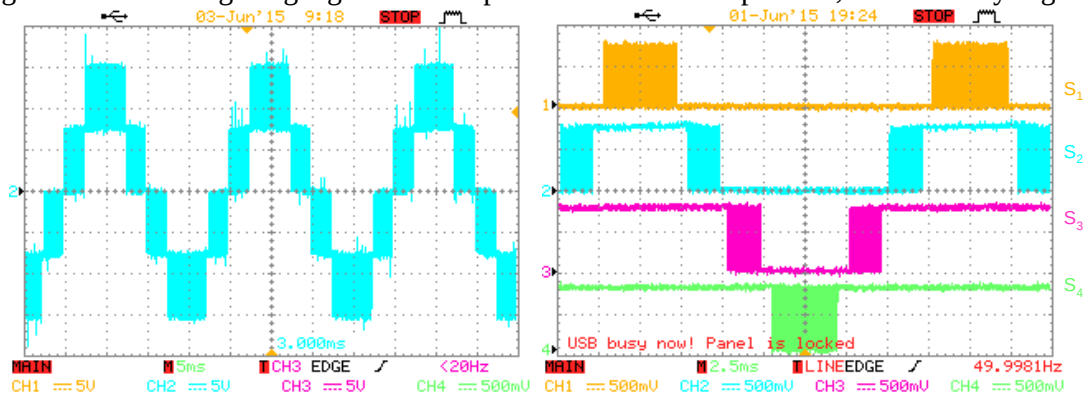

Figure 3: Generated output voltage at no load (left), as well as the corresponding PWM patterns (right).

Use of the analog outputs

One of the objectives of the project is to develop estimators for the fives currents that are drawn by the 5L-NPC on the DC busses. These values may be useful in order to help improve the control of these busses in a more complex application, such as presented in [1, 2]. It is desired that these estimators are based on sliding average values of the duty cycles, as well as the output current. The following code shows the appropriate computations:

```
I1c = Iout * Duty_A;              // 1st stage current (+2U)
I2c = Iout * (Duty_B-Duty_A);     // 2nd stage current (+U)
I3c = Iout * (Duty_D-Duty_C);     // 3rd stage current (-U)
I4c = Iout * (1-Duty_D);          // 4th stage current (-2U)
```

In order to evaluate the accuracy of these estimators, the corresponding current estimations are visualized on an oscilloscope, and compared with the actual current measurements:

```
// Display the following sampled values using the DAC outputs:
SetDACVoltage(0, I1);             // Actual measurement, top bus current
SetDACVoltage(1, I1c);            // Estimated valued, top bus current
SetDACVoltage(2, I1-I1c);         // Estimation error, top bus current
SetDACVoltage(3, I2);             // Actual measurement, second bus current
```

The obtained results are plotted in Figure 3. This approximately corresponds to a maximum relative estimation error of about 20%. This performance is largely sufficient for the needs of most voltage balancing strategies for the DC busses.

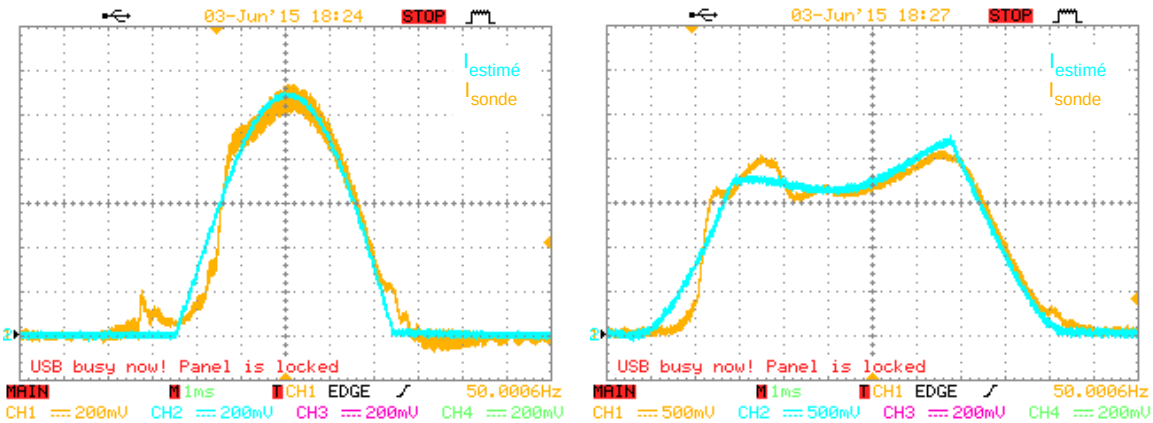

Figure 3: Performance evaluation comparing the estimated value with the actual measurements. (a) current Id12, (b) current Id11

References

[1] A. Rufer. *A Five-Level NPC Photovoltaic Inverter with an Actively Balanced Capacitive Voltage Divider*. Proceedings of PCIM Europe 2015, Nuremberg, May 2015.
[2] A. Rufer, N. Koch, N. Cherix. *Control of the Actively Balanced Capacitive Voltage Divider for a Five-Level NPC Inverter - Estimation of the Intermediary Levels Currents*. Proceedings of PCIM Europe 2016, Nuremberg, May 2016.
[3] Thomas A. Lipo, D. Grahame Holmes. *Pulse Width Modulation for Power Converters: Principles and Practice*. John Wiley Sons, 2003.
[4] imperix SA. *BoomBox*, http://imperix.ch/products/control/boombox/intro.
[5] N. Cherix, S. Delalay, P. Barrade, *Fail-safe Modular Control Platform for Power Electronic Applications in R&D Environments*, EPE 2013, Lille, September 2013.