

SPRING-SUMMER 2027

STUDENT PROJECT PROPOSALS

DEVELOPMENT PROJECTS IN EMBEDDED SYSTEMS

ACCELERATED PORTING OF C++ CONTROL ALGORITHMS TO FPGA

- Motivations:** Power converters based on wide-bandgap devices need control loops with sub-microsecond latency, which often means moving C++ control code from the CPU into the FPGA fabric. With high-level synthesis (HLS), every modification triggers a full place-and-route that can take up to an hour, which breaks the rapid-prototyping workflow imperix users expect. This project investigates which execution architectures and tool flows offer the best trade-off between iteration speed and real-time performance.
- Objectives:** Using Vitis HLS as the baseline, survey the available solutions for executing C++ control algorithms in the FPGA fabric, and evaluate the most promising ones on representative power converter control algorithms. Candidates include HLS combined with Dynamic Function eXchange or incremental implementation or pre-implemented blocks assembled with RapidWright, a standard MicroBlaze soft processor, and Very Long Instruction Word (VLIW) or Coarse-Grained Reconfigurable Array (CGRA) overlays. Compare the solutions in terms of compile time, control latency and jitter, maximum execution rate, FPGA resource and ease of integration into the imperix toolchain. Validate the approach on a real converter controlled by the B-Box 4.
- Skills:** Prior experience with FPGA design and C++ is essential. Knowledge of HLS tools is a plus.

FAST POWER-UP OF SOC-BASED CONTROLLERS

- Motivations:** Imperix controllers are built around Zynq 7000 and Zynq UltraScale+ SoCs, combining CPU cores running embedded Linux or bare-metal code with FPGA logic. Their boot sequence currently takes ~30 seconds. For embedded applications such as power converters built around the B-Board PRO, being operational in less than two seconds after power-up would simplify system start-up and fault recovery.
- Objectives:** Measure the duration of each boot stage on both platforms and identify the main contributors. Evaluate and implement documented optimization techniques, such as faster boot media configuration, bitstream compression, skipping the second-stage bootloader with U-Boot's Falcon mode, kernel and root file system reduction, and deferred initialization of non-critical services. Investigate a staged boot in which the FPGA and the real-time control become operational first, while Linux completes its boot in parallel. Finally, reduce the time to operation by at least an order of magnitude, targeting less than two seconds after power-up, and document the remaining trade-offs.
- Skills:** Experience with embedded Linux is essential. Knowledge of SoC architectures, bootloaders or FPGA configuration is a plus.

REDUNDANT COMMUNICATION FOR DISTRIBUTED CONTROL IN POWER ELECTRONICS

- Motivations:** The imperix RealSync protocol connects multiple controllers over fiber optics to extend their I/Os and implement distributed control algorithms. It distributes a common high-frequency clock across the network, so that all modulators share the same clock domain with an accuracy of $\pm 2\text{ns}$. However, RealSync currently supports only a tree topology with no redundancy, so a single device failure brings the whole system into a fault state.
- Objectives:** Review the literature on network redundancy and identify the topology best suited to RealSync. For each option, determine how many device failures it can tolerate, whether data should be re-routed or broadcast, and whether the number of fiber-optic ports per device limits the achievable redundancy. Implement the selected solution in the FPGA. Upgrade the clock distribution mechanism so that each device can seamlessly

switch to an alternative reference clock when a link fails, and quantify the resulting loss of synchronization accuracy. Evaluate the performance trade-off against the current mode of operation, and validate the work on a realistic real-time control network using numerous imperix controllers.

Skills: Previous experience with FPGA design is essential. Knowledge of communication networks or clock synchronization is a plus.

SUB-MICROSECOND GLOBAL TIME SYNCHRONIZATION FOR DATA ACQUISITION

Motivations: Lab experiments in power electronics and power systems increasingly combine imperix controllers with third-party equipment such as power analyzers, grid emulators or phasor measurement units. These are often synchronized to a global time reference, typically derived from GPS. The IEEE 1588 Precision Time Protocol (PTP) over Ethernet and the IRIG-B time code are the most common ways to distribute such a reference, and both can reach sub-microsecond accuracy.

Objectives: Implement a time synchronization module on a Zynq UltraScale+ MPSoC based controller. It should lock onto either a PTP grandmaster, using the Hardware Time Stamping Unit (TSU) of the Ethernet controller, or an IRIG-B signal decoded in the FPGA. Survey other relevant sources, such as the pulse-per-second output of GNSS receivers. Synchronize the FPGA-based acquisition system to the selected source, and update the existing data acquisition pipeline to use it as the absolute timestamp base for all measurements. Quantify the achieved precision of each source through experimental testing.

Skills: Previous experience with FPGA design is essential. Experience with SoC and embedded Linux is a plus.

DESIGN AND IMPLEMENTATION OF A PHASOR MEASUREMENT UNIT (PMU)

Motivations: Phasor Measurement Units (PMUs) measure voltage and current phasors synchronized to an absolute time reference, enabling wide-area monitoring of power systems. They are also gaining academic interest for distributed generation in low- and medium-voltage grids. Imperix would like to let researchers experiment with PMUs directly on its controllers, with standard-compliant data streaming and live visualization.

Objectives: Implement the acquisition and timestamping of measurement data on an imperix controller, based on an absolute time reference distributed for instance via a GPS receiver, IRIG-B or PTP. Develop estimation algorithms for phasors, frequency and rate of change of frequency, and evaluate them against the accuracy requirements of the IEC/IEEE 60255-118-1 standard. Stream the resulting synchrophasors according to IEEE C37.118.2 and IEC 61850-90-5, and verify interoperability with a third-party phasor data concentrator. Develop a graphical PMU widget for the Cockpit GUI builder. Finally, validate the complete system experimentally on a laboratory grid setup.

Skills: Familiarity with C/C++, Python and embedded Linux is recommended. A background in power systems or signal processing is a plus.

YOUR PROFILE

An internship with us will suit you if:

- You are a PhD, MSc, or BSc student.
- You are looking for a 4-to-9 months on-site internship in Sion, Switzerland.
- You are seeking to work in a dynamic, fast-paced environment.
- You are self-motivated and capable of working both individually and as part of a team.
- You expect attentive supervision of your work from highly qualified engineers.
- You are looking for a position that values and makes room for your initiatives.
- You appreciate a young and friendly environment that is also serious and professional.

If you are interested in doing an internship with us, please send your CV along with a cover letter explaining your motivations and what you would bring to the team. We read every application carefully and reply within 10 days to the profiles that interest us.

Only complete applications are considered, and generic or obviously machine-generated letters are not.

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ABOUT US

Imperix is a leading global provider of high-performance control solutions and rapid prototyping hardware engineered specifically for power electronics. Founded in 2013 as a spin-off from the Swiss Federal Institute of Technology (EPFL), the company accelerates innovation by bridging the gap between numerical simulation and physical implementation.

At the core of the Imperix ecosystem is the flagship B-Box controller family, which unites robust digital processing, the intuitive Cockpit software, and automated code generation from Simulink and PLECS. These control development solutions are complemented by a comprehensive hardware portfolio encompassing modular power stages, high-fidelity sensors, fully integrated inverters, as well as hardware and software interfaces for real-time HIL/PHIL simulation. Together, these tools empower top-tier industrial and academic R&D teams to safely test advanced control algorithms on real hardware within minutes, drastically reducing time-to-market and time-to-publication.

Headquartered in Sion, Switzerland, Imperix serves a prestigious client base across more than 50 countries. By delivering specialized, modular tools for power conversion, smart grids, motor drives, electric mobility, and energy storage, Imperix stands at the forefront of the technology enabling the global energy transition.