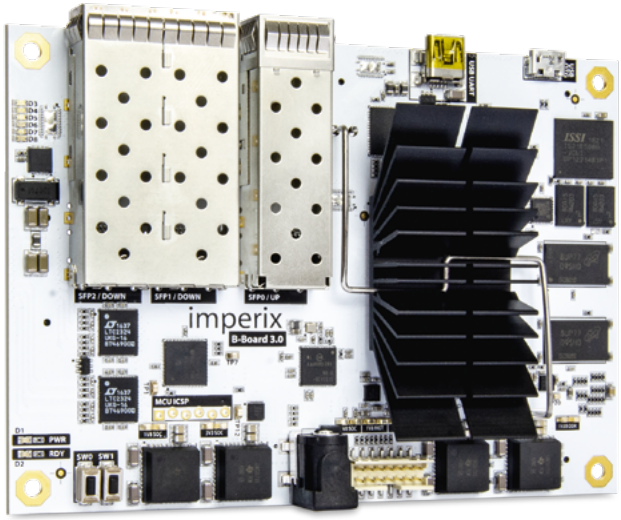
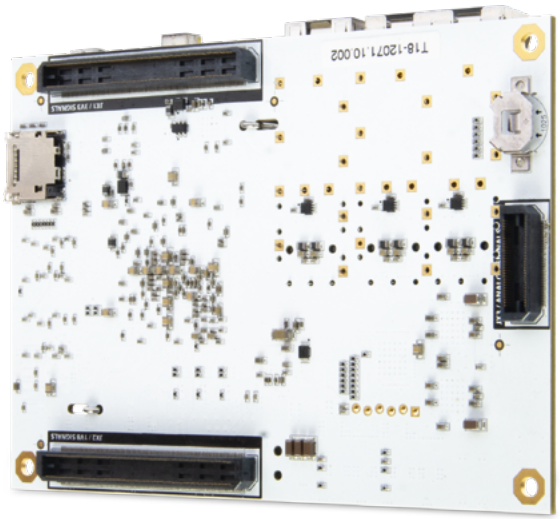
B-Board PRO

Embeddable controller

The B-Board PRO is an advanced controller designed for series-manufactured products.





GENERAL DESCRIPTION

The B-Board PRO is the core of the B-Box RCP rapid control prototyping platform, which can also be used a standalone unit, directly within series-manufactured products.
Thanks to the exact equivalence between B-Box RCP and B-Board PRO, users can benefit from the increased flexibility of the prototyping controller for research, while using a smaller and more cost-effective variant during production. In practice, code that has been developed on B-Box can be ported instantly on B-Board, hence offering a total transparency between both platforms. This approach significantly reduces the time needed for engineers to make the transition between the laboratory and the field, eventually reducing the time to market.

TYPICAL APPLICATIONS

The B-Board PRO is designed for use within the most demanding power electronic systems, which require intensive R&D, as well a short development cycles. Its attractive computing performance and large flexibility also make it the perfect fit for systems that feature complex control algorithms.
Finally, its excellent PWM resolution makes it ideally suited for use with wide band gap devices such as SiC or GaN.

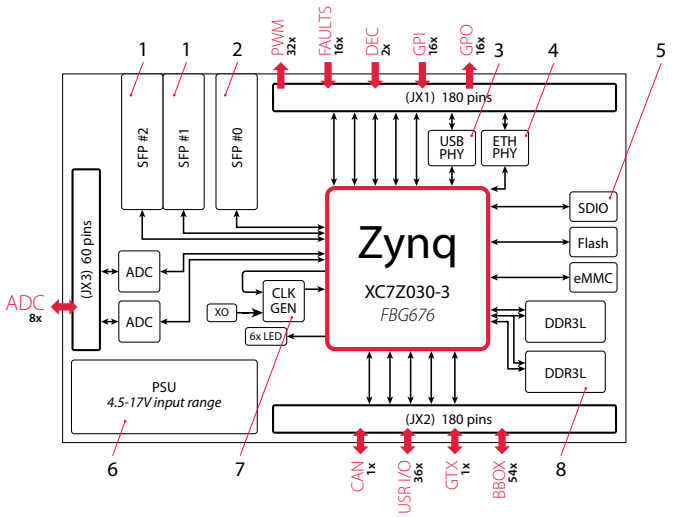
KEY FEATURES AND SPECIFICATIONS

The B-Board PRO has been designed from the start for optimal operation in synchronous sampling applications. Indeed, it offers a large reconfigurability of timings and guarantees a very strict management of all phase shifts, from analog inputs to PWM outputs, including operation in networked control configurations.
Excellent computational performance is guaranteed, thanks to a dual-core ARM Cortex processor and a Kintex-grade FPGA, supporting closed-loop control applications up to hundreds of kHz!
Networked configurations of up to 64 controllers and hundreds of I/Os are supported by *RealSync*, a proprietary technology that guarantees sub-µs communication latency and ns-scale synchronization accuracy. The main system specifications are:

- Dual-core 1 GHz ARM processor
- Kintex-grade FPGA (user programmable)
- Advanced pulse-width modulators (PWM)
- 4 ns PWM resolution
- 140 user I/Os per unit
- 86 x 124 x 22 mm form factor

DEVICE DESCRIPTION

1) SFP Interconnect – DOWN links
2) SFP Interconnect – UP link
3) USB OTG (on bottom BSH)
4) Gigabit Ethernet (on bottom BSH)



5) Onboard memories:
   – SD card slot
   – 32 MB Flash (program)
   – 8 GB Flash (logging)
6) Wide input range on-board power supply
7) SFP clocks management
8) DDR memory (1 GB)

Fig. 1. Simplified structure of the B-Board processing module.

MAIN SPECIFICATIONS

Component	Specification
System on chip	Xilinx Zynq XC7Z030-3FBG676E
Processing system	ARM Cortex A9 1 GHz x2 1GB DDR3
Programmable logic (FPGA)	Kintex 7 125K (user programmable)
Storage	Flash 16MB x2 micro SD + eMMC 8GB
Communication	USB OTG x1 Ethernet 1Gbps x1
	USB 2.0 high speed console x1 SFP+ 5 Gbps x3
Power supply	4.5–17 VDC (15 W)
Operating temperature range	0 – 80 °C

Component	Specification
PWM outputs	Electrical (3V3) x32 Various modulators 4 ns resolution
Analog inputs	16 bits, simultaneous sampling x8 2 Msps (maximum speed) / 500 ksps (B-Box compatibility mode)
Incremental decoder inputs	3-pins (A,B,Z) x4 Shared with GPI inputs
Fault inputs / outputs	Digital (3.3V) x16 Electrical interlock (3.3V) x1
General-purpose digital inputs (GPI)	Electrical (3.3V) x16
General-purpose digital outputs (GPO)	Electrical (3.3V) x16
User High-speed I/Os	FPGA direct (3V3) x36

Table 2. Main system specifications for B-Board PRO.

MAXIMUM I/O CAPABILITIES

Component	Characteristics	Single (1 unit)	Networkedd (64 units)
Analog inputs	2 Msps, ± 5 V differential inputs	8	512
PWM outputs	Electrical, >500 Mbps	32	2048
General-purpose digital outputs (GPO)	Electrical, >100 Mbps	16	1024
General-purpose digital inputs (GPI)	Electrical, >100 Mbps	16	1024

Table 3. Maximum I/O count per B-Board PRO and in networked configuration.

ENVIRONMENTAL CONDITIONS

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
DC input voltage		4.5	12	17	V
Power consumption		5	7.5	32	W
EMC performance	Radiated IEC61000-3-2 class A / Conducted IEC61201-3 class A / Burst IEC61000-4-4 Level 4	pass			
Operating temperature	Operation above 55°C requires active cooling of the heatsink (forced air).	0		80	°C
Storage temperature		-25		85	°C
Temperature change rate		-0.5		0.5	°C/min
Relative humidity	Non-condensing	0		100	%
Absolute humidity	Non-condensing	1		29	g/m³

Table 4. Environmnental specifications for the B-Board PRO.

LOGICAL STRUCTURE

The B-Board PRO is built on an association of two CPU cores and dedicated peripherals implemented in programmable logic. The distribution of tasks is as follows:

» CPU0: Running on Linux, the first core is responsible for loading the application code, supervising the system execution and managing the data logging.
» CPU1: Running on BBOS (lightweight secured proprietary operating system), the second core executes the application-level control code developed by the user.
» FPGA: The programmable logic area contains all the application-specific peripherals. By default, the corresponding firmware is fixed.

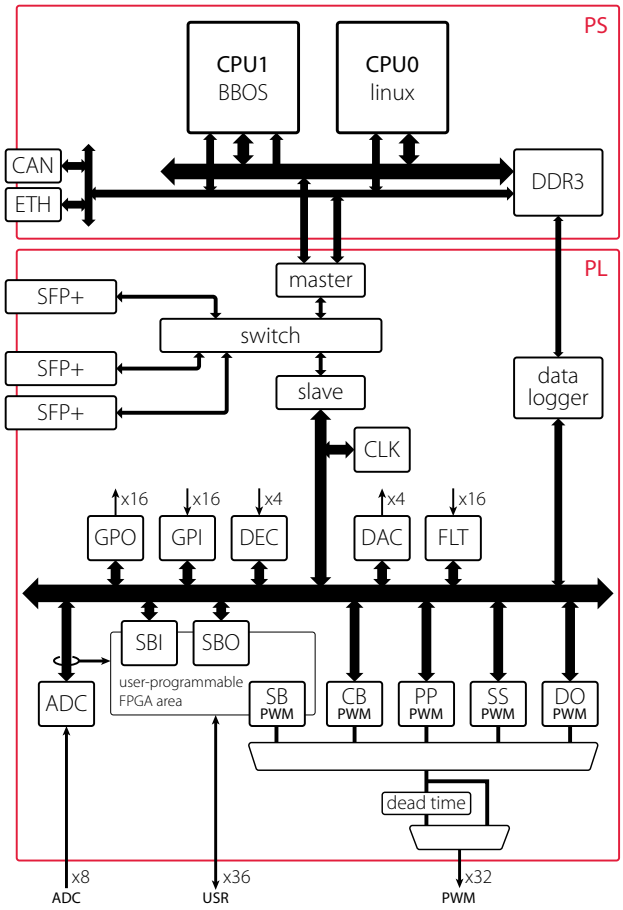


Fig. 2. Functional overview of the B-Board PRO controller.

The pre-implemented FPGA peripherals are as follows:

» CLK: Provides clock generators with up to four separate time-bases that can be used with other peripherals.
» ADC: Acquires data from the 8 analog input channels located on board.
» DAC: Updates the 4 analog output channels.
» SBI: Provides easy-to-use access for inbound data traffic from the user-programmable area (sandbox).
» SBO: Provides easy-to-use access for outbound data traffic from the user-programmable area (sandbox).
» DEC: Allows the decoding of signals produced by up to four incremental encoders for motor drive applications.
» CB-PWM: Contains 32 fully-configurable carrier-based modulators (conventional sampled PWM).
» SS-PWM: Implements multilevel modulation for modular converters using a Sort-&-Select voltage balancing technique such as commonly used in Modular Multilevel Converters (MMC). It achieves the balancing of floating capacitors, while maximizing the ration between waveform performance and average switching frequency.
» PP-PWM: Provides hardware support for the generation of Programmed Patterns. It is useful for techniques such as modulation with Selective Harmonic Elimination (SHE) or Optimized Pulse Patterns (OPP) in general.
» DO-PWM: Offers a Direct Output operation, allowing to force a specific lane state (0 or 1). This is useful for control techniques such as Model Predictive Control (MPC) or Direct Torque Control (DTC).
» SB-PWM: Provides access to the PWM outputs from the user-programmable area (sandbox).
» GPO: Offers 16 General-Purpose Outputs.
» GPI: Offers 16 General-Purpose Inputs.
» FLT: Offers 16 configurable fault inputs. These inputs can also be used as general-purpose inputs.
» USR: Provides a direct access to the 36 fully-configurable high-speed I/O lanes.
» ETH: Supports data exchanges on Ethernet (TCP/UDP).
» CAN: Provides connectivity with CAN peripherals.

ANALOG INPUTS

The B-Board PRO has two LTC2324-16 16 bits full-differential analog-to-digital converters from Linear Technologies, with a total of 8 channels. The devices guarantee simultaneous sampling on all channels. Overall performance specifications are given in Table 5. Timing characteristics are shown in Table 6.

Data transfer to the processing cores is achieved by FPGA and over *RealSync* in case of multi-unit operation. Transfer delays vary with the amount of data (see Fig. 3). The overall delay from sampling to cache memory is therefore the sum of the A/D conversion time plus data transfer delay.

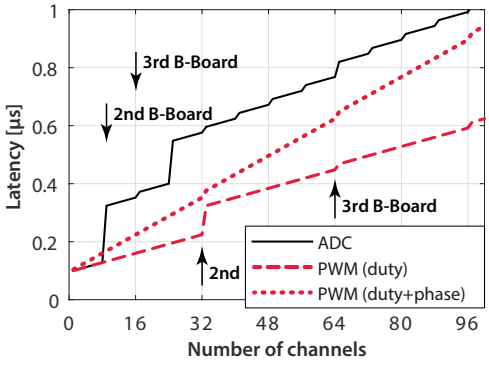


Fig. 3. Data transfer delay, as a function of the number of channels

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Input voltage range	*Differential mode*		*±5.0*		*V*
Max. tolerable voltage	*Both input pins*	*-0.3*		*5.3*	*V*
Power supply voltage		*5.15*	*5.2*	*5.3*	*V*
CMRR	f_{IN} = 500 kHz		*102*		*dB*
THD	f_{IN} = 500 kHz		*-91*		*dB*
Signal–to–noise ratio	f_{IN} = 500 kHz		*82.5*		*dB*
Full-scale error		*-35*	*±12*	*+35*	*LSB*
Input DC leakage current	*Each pin*	*-1*		*+1*	*µA*
Input capacitance	*Each pin*		*10*		*pF*
Power consumption	*On 5.2 V supply*		*160*	*250*	*mW*

Table 5. Performance specifications of the A/D conversion.

For proper operation, the carrier board should be designed such that the following design guidelines are followed:

- **Power supply:** A clean 5.2V power supply must be provided on the JX3 connector in order to supply the ADC chips. This power supply is entirely separated from other on-board power supplies.
- **Protection:** It is recommended to implement overvalue detection mechanisms on the carrier board in order to provide hardware-level protections for the to-be-controlled power converter.
- **ADC driver:** A low-offset wide-bandwidth operational amplifier must be present on the carrier board in order to effectively drive the ADCs. When selecting operational amplifiers, attention must be paid to the following performance characteristics:
  - Settling time (typ. 0.1% < 30 ns)
  - Slew rate (typ. > 250 V/µs)
  - Input offset (typ. < 400 µV)
  - Suitable output voltage range (typ. 0.1 – 4.9V)

  Imperix recommends considering the following components for the carrier board design:
  - THS4551 for a full-differential solution with a single +5.2V power supply. An example is given in Fig. 5.
  - AD8021 for a high-performance solution with power supplies up to ±12V. A recommended schematic with an output for protection thresholds is given in Fig. 6. The input common-mode range is 0.1–3.9V.
  - AD826 or LT1360 for solutions with ±15V power supplies. Other speed / precision trade-offs may also be selected.

FPGA-BASED PERIPHERAL BLOCK

Depending whether the B-Board is used inside the B-Box or in standalone mode, the ADC peripheral block switches between two precisely-matched subsystems. This guarantees that the analog input chain behaves strictly identically in both configurations.

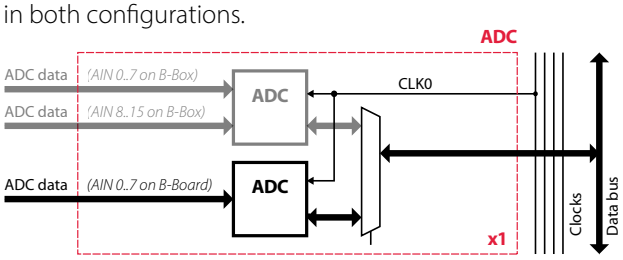


Fig. 4. Internal structure of the ADC peripheral block.

EXPANDING THE ANALOG INPUTS

Using the user-programmable area of the FPGA (see page 13), external ADC chips may be connected to the B-Board PRO in order to increase the number of analog channels.

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Aperture delay			*500*		*ps*
Transient response	*Full-scale step*		*30*		*ns*
Sampling jitter	*Same B-Board*		*±2.1*		*ns*
	Across all B-Boards		*±3.6*		*ns*
Conversion time	*Retro-compatible mode with B-Box RCP hardware < 3.5 (commercialized 2020)*		*1.98*		*µs*
	Full-performance mode (non-transparent with B-Box HW < 3.5)		*220*		*ns*
Data transfer delay		*See Fig. 3.*			*ns*
Sampling rate	*Retro-compatible mode with B-Box RCP hardware < 3.5 (commercialized 2020)*	*0.0*		*500*	*ksps*
	Full-performance mode (non-transparent with B-Box HW < 3.5)	*1.0*		*2.0*	*Msps*

Table 6. ADC timing specifications

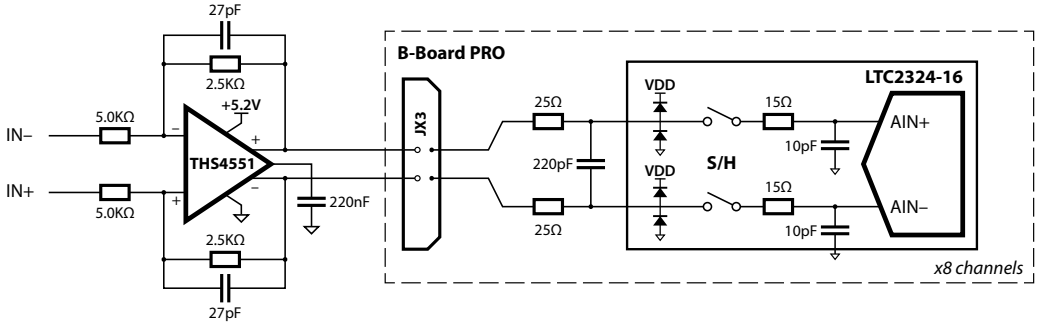


Fig. 5. Recommended carrier schematic for the ADC signals with +5.2V power supply.

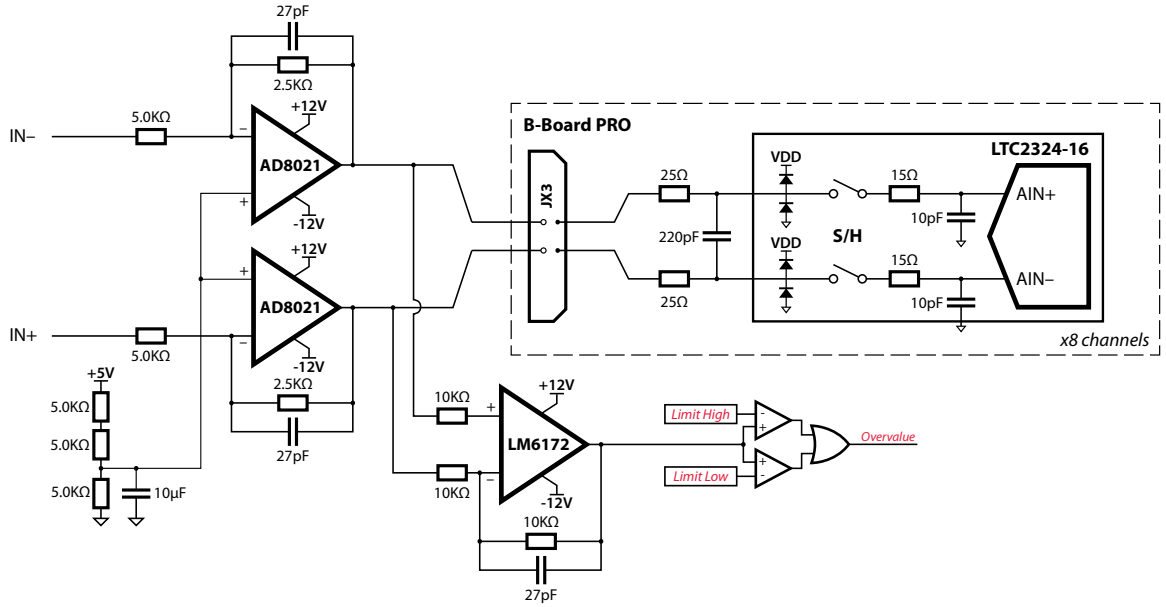


Fig. 6. Recommended carrier schematic for the ADC signals with separate ±12V power supplies.

POWER SUPPLIES

Unlike most other piggy-back control boards, the B-Board already embeds all power supplies, so that only two supply voltages are needed:

» **Digital circuits:** A **4.5–17V** DC power supply must be provided as the main power supply. Voltages of 5V, 12V and 15V are therefore all applicable with B-Board PRO, offering a large flexibility for integration within existing equipment. This power supply is subdivided on board to generate lower voltages such as 1.0V, 1.2V, 1.8V, 3.3V.

» **Analog circuits:** Another **5.2V** DC power supply must be provided.[1] It is exclusively used by the analog-to-digital converters. It may therefore be neglected in case the on-board ADCs are not used.

POWER SUPPLY SEQUENCING

In order to prevent excessive current flows during the power-up process (that may endanger the Zynq or other components), the carrier board should be designed such that the following sequence is observed:

1) Allow internal logic of the Zynq to power up first. Wait until the B-Board raises its **BB_RDY** flag for applying any voltage larger than 1.8V to the B-Board I/O pins.

2) In case some devices require a particular power-up sequence on the carrier board or may be endangered by voltages applied from the B-Board PRO, the **MB_RDY** flag must be held low until this particular sequence is completed. Alternatively, **MB_RDY** can be left floating as it is weakly pulled up on the B-Board.

3) When the **MB_RDY** flag is sensed high, the B-Board finishes its power up sequence by powering the previously-gated 3.3V devices as well as Zynq transceivers.

4) Independently, once he **BB_RDY** pin is held high, 3.3V circuits can be safely powered up on the carrier board without endangering the Zynq.

1 The 5.2V power supply may be used at lower voltages (e.g 4.75–5V) with limitations on the analog input voltage range. Please contact support@imperix.ch to learn about the technical limitations before considering this option.

BOOTING SEQUENCE

Once all power supplies are properly powered up, the Zync initiates its booting procedure, which takes around 20s. The overall sequence can be followed using the green LEDs D3-D5, which indicate further details.

RDY	D3	D4	D5	Status	Duration
0	0	0	1	Core power up in progress	60 ms
0	0	1	0	3V3 power up in progress	50 ms
0	1	0	0	Transceiver power up in progress	150 ms
0	1	1	0	Clock configuration in progress	60 ms
0	1	1	1	Zynq booting in progress	60 ms
1	0	0	0	Operating system loading in progress	18-25 s
B[2]	0	0	0	Network discovery in progress	2-20 s
1	1	0	0	Master standby (successfully booted)	N/A
1	B[3]	0	0	Slave standby (successfully booted)	N/A
1	X	1	0	User code running, PWM disabled	N/A
1	X	1		User code running, PWM enabled	N/A
1	B[4]	B[4]	B[4]	Firmware upgraded. Please reboot !	inf.

Table 7. LED indicators (green) during the power up sequence.

STATUS LEDS AT BOOT

Two on-board LEDs indicate the execution state of the overall power up and boot sequence :

» D1 / PWR turns blue when input power is available on the B-board. It should therefore be always on.

» D2 / RDY turns blue when the B-Board has successfully completed the power up and booting sequence.

In case anything goes wrong during the booting sequence, an error code is displayed using the D6-D8 LEDs.

RDY	D6	D7	D8	Status
0	0	0	1	Power failure during the powering of the core voltage
0	0	1	0	Power failure during the powering of the 3.3 V supply
0	0	1	1	Power failure during the powering of the transceivers
0	1	0	X	Failure during the clock configuration
0	1	1	0	Failure during the Zynq booting process
0	1	1	1	Power failure after booting (i.e. during normal operation)
0	0	0	0	No error
1	X	X	X	Control of LEDs transferred to Zynq

Table 8. Error codes (red) applicable during the power up sequence.

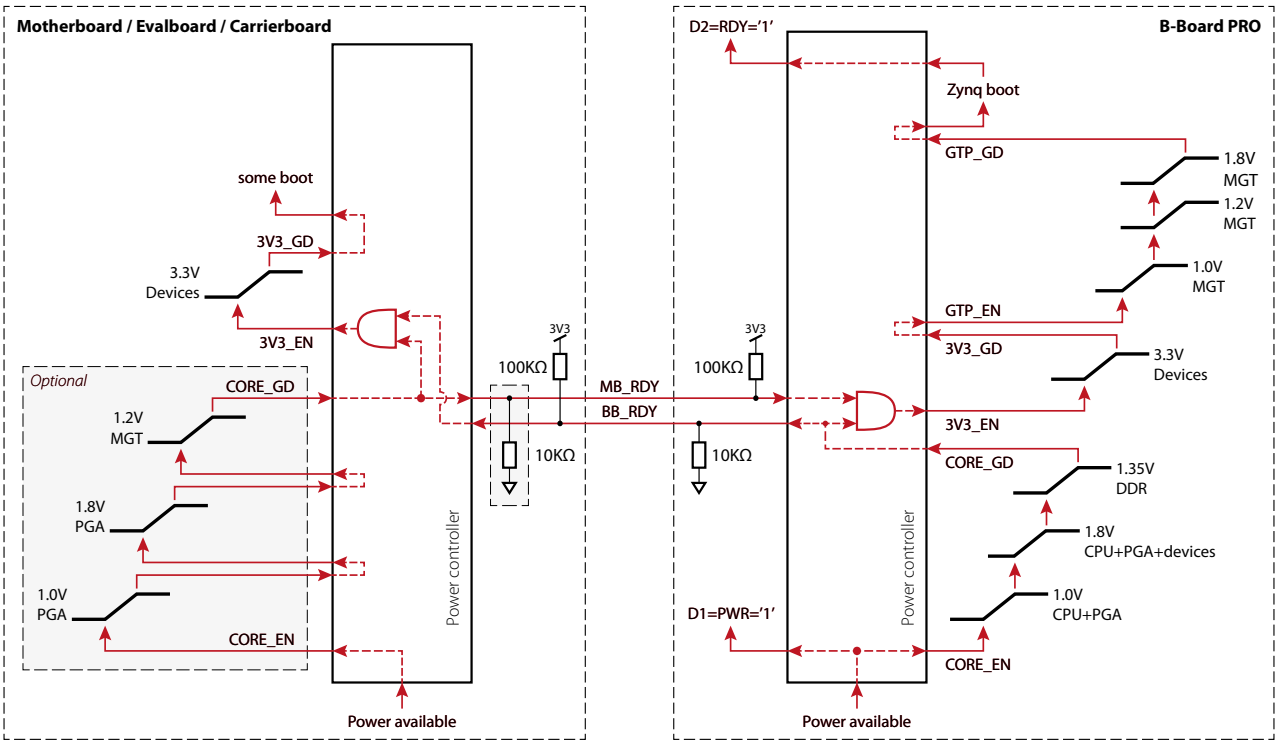


Fig. 7. Power sequencing scheme of the B-Board PRO.

2 During synchronization, RDY is permanently blinking at 4 Hz.
3 When connected as a slave, D3 is shortly blinking at 2 Hz as many ticks as the Device ID.
4 After a new firmware is flashed, all D3-D5 LEDs are permanently blinking until the board is rebooted.

DIGITAL I/O SIGNALS

All digital inputs are available on the two high-speed connectors JX1 and JX2. The following functions are available:

- PWM: Pulse-width modulated signals (32 bits)
- GPO: General purpose outputs (16 bits)
- GPI: General purpose inputs (16 bits)
- FLT: Fault feedback inputs (16 bits)
- USR: Fully-configurable input / output bus (32 + 4 bits)
- CAN: Controller Area Network communication (2 bits)
- ETH: Ethernet MDI signals from onboard PHY (8 bits)

The location and voltage level of the related pins is summarized in Table 9.

> WARNING:
> Always pay attention to the **logic voltage level** of each signal. Refer to Table 9 for detailed information. Unexpected behavior or damages may occur in case inappropriate voltage is applied to the Zynq or any other circuit.

Peripheral	Bit lanes	Level	Main functions and bus width	Alternate function	Connector	Internal topology	Typ. speed
GPI	GPI 0-7	3.3 V	General-purpose inputs (16 bits)	Incremental decoder	JX 2	Direct to Zynq	400 Mbps
	GPI 8-15	3.3 V		Incremental decoder	JX 1	Level shifted to 1.8V on B-Board	150 Mbps
GPO	GPO 0-7	3.3 V	General-purpose outputs (16 bits)		JX 2	Direct to Zynq	400 Mbps
	GPO 8-15	3.3 V			JX 1	Level shifted to 1.8V on B-Board	150 Mbps
PWM	PWM 0-15	3.3 V	Pulse-width modulated signals (32 bits)	High-speed DOUT	JX 2	Direct to Zynq	400 Mbps
	PWM 15-31	1.8 V		High-speed DOUT	JX 1	Direct to Zynq	500 Mbps
FLT	FLT 0-15	1.8 V	Fault feedback signals (16 bits)	High-speed DIN	JX 1	Direct to Zynq	500 Mbps
USR	USR 0-35	3.3 V			JX 2	Direct to Zynq	400 Mbps
CAN	CAN TX/RX	3.3 V	Controller Area Network signals		JX1	Direct to Zynq	1 Mbps
ETH	PHY 0-4	N/A	Ethernet signals (PHY MDI)		JX1	Direct to on-board PHY	1 Gbps

Table 9. General specifications of the digital signals available on the high-speed connectors.

ELECTRICAL PWM OUTPUTS (PWM)

On B-Board, 32 PWM lanes are available. The first 16 lanes (i.e. #0–15) are available at 3.3V, while the remaining lanes are based on 1.8V logic. Two consecutive PWM lanes are by default associated to form a PWM channel with three possible configurations:

- PWMH + PWML: high- and low-side signals with configurable dead time between their '1' states.
- PWM + ACTIVE: PWM and switching authorization signals, i.e. one modulated switching signal and one flag for blocking / unblocking the operation.
- INDEPENDENT: each PWM lane is tied to its own PWM modulator. No dead time is enforced.

Due to the mixed logic voltage levels, the recommended carrier-board schematic includes the level shifting of 1.8V signals to 3.3V (or other) logic voltage.
In addition, in order to prevent any possible logic high value during the FPGA boot-up sequence, all PWM signals must be pulled-down with a relatively strong value. When desired, the output enable signal of the level shifter may also be used to gate the PWM signals, possibly by combining the nFLT_OUT signal of the B-Board with some locally-generated fault signal(s).

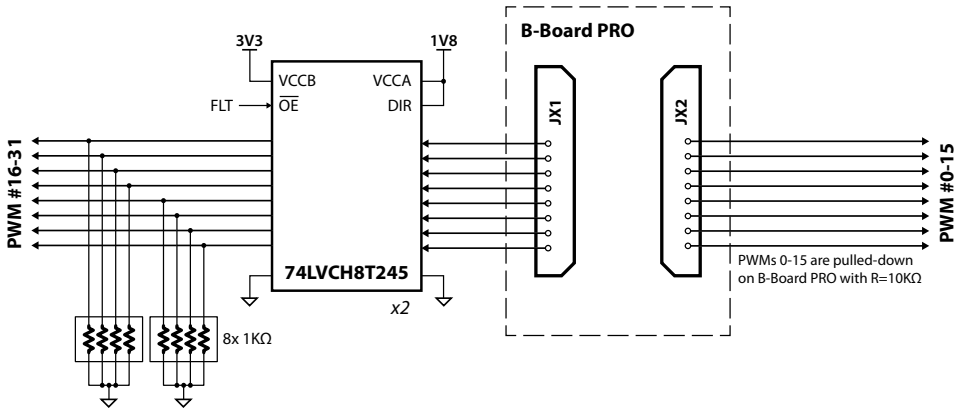


Fig. 8. Recommended carrier-board schematic (with level shifting) for the PWM signals.

Electrical PWM outputs are engineered to provide a very high accuracy of timings. This is valid inside a PWM channel, across

the whole bus and even across all networked B-Boards. Table 10 shows the performance specifications.

Characteristic	Channels	Test conditions	Min.	Typ.	Max.	Unit
Operating voltage	PWM 0-15 (3.3V)		3.0	3.3	3.6	V
	PWM 16-31 (1.8V)		1.5	1.8	2.0	V
Propagation delay asymmetry	PWM 0-15 (3.3V)	Any two signals on same B-Board			± 1.6	ns
	PWM 16-31 (1.8V)				± 2	ns
	Any PWM	Any two signals on same B-Board			± 2.5	ns
		Any two signals across all networked B-Boards			± 4.5	ns
Relative jitter	Any PWM	Any two signals on same B-Board			± 0.4	ns
		Any two signals across all networked B-Boards			± 0.7	ns

Table 10. Performance specifications of the PWM outputs.

GENERAL-PURPOSE OUTPUTS (GPO)

16 outputs are available, spread between JX1 and JX2. They are tied to the GPO block. All GPO signals are at 3.3 V.

Characteristic	Min.	Typ.	Max.	Unit
Operating voltage		3.3	3.5	V
Current drive capability			12	mA
Max signal rise / fall time			± 3	ns
Propagation delay asymmetry, same B-Board			± 2.5	ns
Propagation delay asymmetry, any B-Board			0.2*N	us

Table 11. Performance specifications of the GPO outputs.

In some cases, it may be needed to shift the GPO signals to another logic voltage level and / or to improve the current drive capability of each bit. In that case, a similar circuit as shown in Fig. 8 may be considered. Furthermore, the same pull-down resistors may be useful as well.

GENERAL-PURPOSE INPUTS (GPI) AND INCREMENTAL DECODER INPUTS (DEC)

16 outputs are available, spread between JX1 and JX2. They are statically tied to the GPI block as well as the DEC block. All GPI signals are at 3.3 V.

Characteristic	Test conditions	Value	Unit
Maximum tolerable input voltage	3.3 V	3.6	V

Table 12. Performance specifications of the GPI/DEC inputs.

Pin	GPI signal	DEC signal	Pin	GPI signal	DEC signal
JX2 / 105	GPI 0	A0	JX1 / 79	GPI 8	A1
JX2 / 106	GPI 1	B0	JX1 / 80	GPI 9	B1
JX2 / 107	GPI 2	Z0	JX1 / 81	GPI 10	Z1
JX2 / 108	GPI 3	A2 or $\overline{A0}$	JX1 / 82	GPI 11	A3 or $\overline{A1}$
JX2 / 110	GPI 4	B2 or $\overline{B0}$	JX1 / 84	GPI 12	B3 or $\overline{B1}$
JX2 / 111	GPI 5	Z2 or $\overline{Z0}$	JX1 / 85	GPI 13	Z3 or $\overline{Z1}$
JX2 / 112	GPI 6	N/A	JX1 / 86	GPI 14	N/A
JX2 / 113	GPI 7	N/A	JX1 / 87	GPI 15	N/A

Table 13. Signal assignment for the GPI / DEC inputs.

FAULT FEEDBACK INPUTS (FLT)

16 digital input lanes are available as fault feedback signals (e.g. for gate drivers). These signals are tied to the fault manager block (FLT), but can also be used as digital inputs from the application software. An additional pre-implemented fault inter-locking also exists. Further details are presented in section "Fig. 10. Recommended carrier schematic for the ETH signals." on page 9.

Characteristic	Min.	Typ.	Max.	Unit
Response delay to blocking of PWM signals		50	60	ns
Operating voltage	1.5	1.8	2.0	V

Table 14. Performance specifications of the fault feedback inputs.

The FLT input lanes are pulled down inside the Zync chip. As such, faults are by default inactive, unless the polarity of the signals is changed to active low by software.

USER-CONFIGURABLE I/O BUS (USR)

The B-Board PRO features a high-speed bus of 36x bidirectional I/Os that is directly accessible from the user-programmable area (inside the Zynq chip). This area, also designated as sandbox offers easy-to-use access from / to the processing cores through the dedicated SBI and SBO blocks.

Characteristic	Min.	Typ.	Max.	Unit
Operating data bitrate (all lanes)			400	Mbps
Operating voltage	3.0	3.3	3.6	V
Current drive capability			12	mA

Table 15. Performance specifications of the USR bus.

Pins	Name	Dir	Function description
JX2 / 34-37, 39-42	USR 0-7	I/O	Any (e.g. data / address)
JX2 / 9-42, 44-47	USR 8-15	I/O	Any (e.g. data / address)
JX2 / 147-144, 143-139	USR 16-23	I/O	Any (e.g. data / address)
JX2 / 137-134, 132-129	USR 24-31	I/O	Any (e.g. data / address)
JX2 / 153-152, 150-149	USR 32-35	I/O	Any (e.g. data / address / strobes)

Table 16. Signal assignment of the USR bus.

CONTROLLER AREA NETWORK (CAN)

TX and RX signals for CAN communication are available on B-Board PRO. A suitable transceiver is necessary on the carrier board (e.g. SN65HVD232DR).

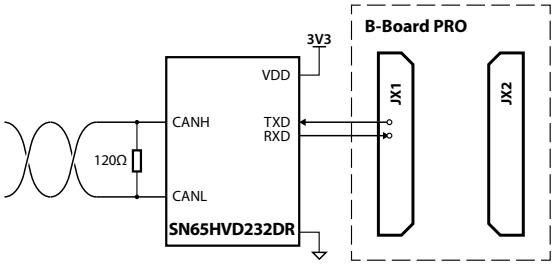


Fig. 9. Recommended carrier schematic for the CAN signals.

Pins	Name	Direction	Function description
JX1 / 176	*CAN TX*	*Output*	*CAN data output*
JX1 / 177	*CAN RX*	*Input*	*CAN data input*

Table 17. Signal assignment of the CAN bus.

ETHERNET COMMUNICATION SIGNALS (ETH)

The utilized PHY is Marvell 88E1512-A0-NNP2I000, which directly provides Ethernet signals on connector JX1, such that only an Ethernet filter is required on the carrier board. Fig. 10 shows the recommended schematic. It is of course possible to use an RJ45 connector with integrated magnetic. Usual high-speed routing techniques used for Gigabit Ethernet connections should preferably be applied. Furthermore, ESD protection measures may be required as well.

Pins	Name	Dir	Function description
JX1 / 20-19	*PHY MDI 0 P/N*	*I/O*	*MDI 0 signals pair*
JX1 / 17-16	*PHY MDI 1 P/N*	*I/O*	*MDI 1 signals pair*
JX1 / 14-13	*PHY MDI 2 P/N*	*I/O*	*MDI 2 signals pair*
JX1 / 12-11	*PHY MDI 3 P/N*	*I/O*	*MDI 3 signals pair*
JX1 / 167	*PHY LED0*	*OUT*	*Status LED 0*
JX1 / 168	*PHY LED1*	*OUT*	*Status LED 1*

Table 18. Signal assignment of the PHY bus.

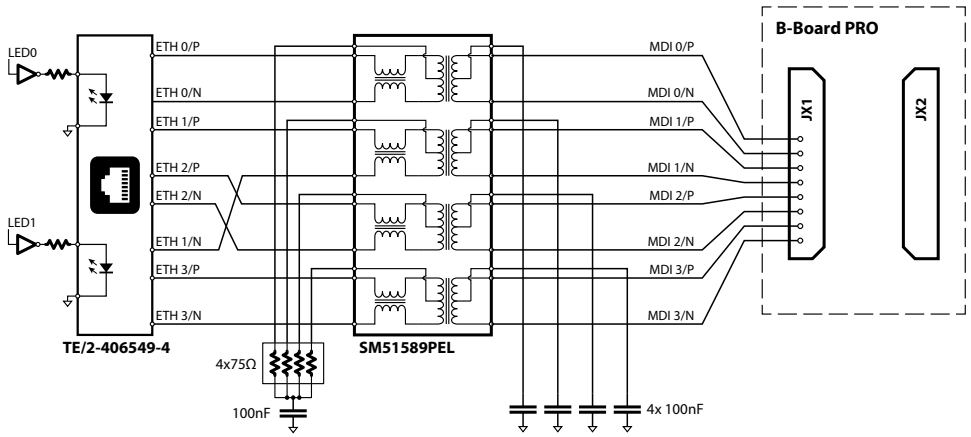


Fig. 10. Recommended carrier schematic for the ETH signals.

FAULT INTERLOCKING SIGNALS

Fault inter-locking allows coordinating emergency mechanisms between multiple B-Boards or with other systems. These mechanisms are bi-directional in the sense that they can inform other devices about an internal fault condition or, reciprocally, receive external trigger signals.
In networked configurations, fault inter-locking is intrinsically available thanks to the *RealSync* protocol (SFP links). The interlock involves one fault input and one fault output (see Table 200).

Characteristic	Trigger	Min.	Typ.	Max.	Unit
Response delay to blocking of PWM signals	*nFLT IN*		*40*	*50*	*ns*
	RealSync		*0.2*N*		*µs*

Table 19. Performance specifications of the inter-locking.

Pins	Name	Direction	Level	Function description
JX2 / 31	*nFLT OUT*	*Output*	*3.3V*	*Critical fault output flag*
JX2 / 32	*nFLT IN*	*Input*	*3.3V*	*Critical fault input flag*

Table 20. Signal assignment for the fault inter-locking signals.

FAULT MANAGER

At the firmware level, all fault signals are grouped inside the fault manager, which manages the overall system execution state and controls the activation of the PWM outputs. The collected fault signals include:

- Dedicated fault input lines FLT 0..15 (JX1)
- Interlock (electrical)

BBOS allows configuring the enabling / disabling of each digital fault input line individually through a configuration mask. All signal values (fault flags) can be read from the corresponding VALUES register.

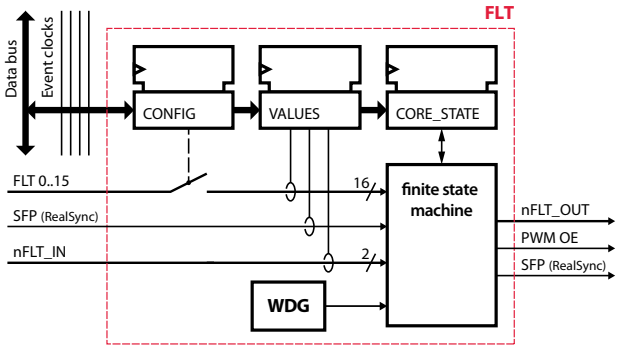


Fig. 11. Internal structure of the FLT peripheral block.

CLOCK AND INTERRUPT GENERATORS

Four independent clock generators are available on B-Board PRO. They allow to configure independent time bases that can be allocated to various FPGA peripherals. This guarantees a very strict management of frequencies and phase-shifts between blocks. Clock generators support glitch-less re-configuration during run-time (variable-frequency). Outputs of clock generators are either interrupt signals or reference clocks for pulse-width modulators. Typical configurations include:

- **Basic example**: Control, modulation and sampling are at the same frequency. All resources are mapped onto the same clock generator. Measurements are made in the middle of the current ripple.
- **Multi-frequency example**: Two distinct converters are switching at different frequencies (e.g. 4 kHz and 5 kHz). Sampling is done at a common multiple (e.g. 20 kHz).
- **Variable-frequency**: One variable-frequency generator is used for modulation. Another frequency generator is used at a constant frequency for sampling and control.

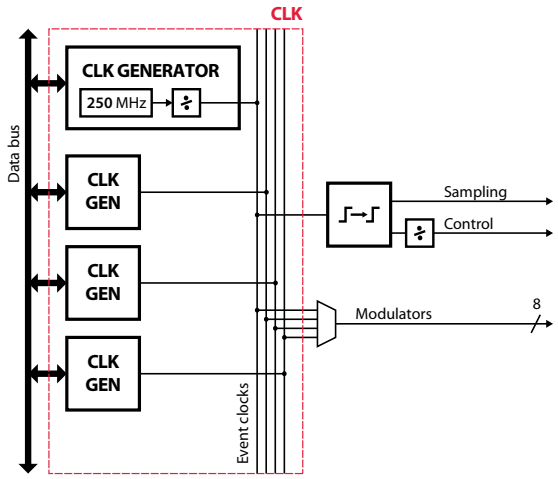


Fig. 12. Internal structure of the CLK peripheral block.

Characteristic	Value
Counter resolution	*4.0 ns*
Counter depth (carrier, prescaler)	*16 bits*
Postscaler value (IRQ subsystem)	*0 – 4095*
Achievable frequency range	*58.2 mHz – 250 MHz*

Table 21. Performance specifications of the CLK peripheral block.

In a multi-device configuration (with networked B-Boards), all clock generators are intrinsically syntonized and automatically synchronized. This way, all phase-dependent operations such as sampling (ADC) or modulation (PWM) are guaranteed to have extremely accurate timings. Achievable performance is shown in Table 222 and illustrated in Fig. 13.

Characteristic	Min.	Typ.	Max.	Unit
Mean deviation, any slave B-Board vs. master	*-2.0*	*0*	*2.0*	*ns*
Phase noise (jitter), any B-Board, 3σ		*±230*		*ps*

Table 22. Synchronization performance of CLK peripheral blocks across multiple B-Boards using *RealSync*.

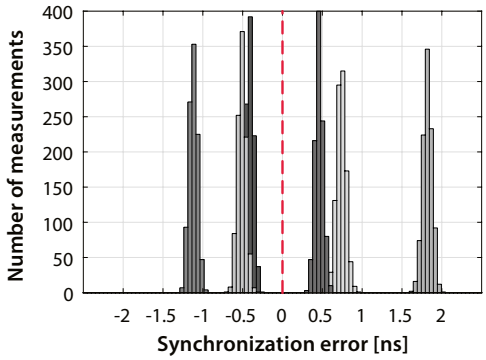


Fig. 13. Relative phase error performance with several B-Boards in a stacked configuration (example with 6 slaves units).

PULSE WIDTH MODULATORS

The B-Board PRO embeds a full PWM signal generation system, featuring five sub-systems. Each of them generates 32 PWM signals. Fig. 14 depicts the corresponding structure:

- **CB-PWM**: Carrier-based modulators (32 channels). Various types of carriers are available, with single or double update rate. The CB-PWM block also provide hardware support for space-vector modulation (SV-PWM).
- **PP-PWM**: Programmed patterns modulators (2x three-phase). They support the implementation of Selective Harmonic Elimination (SHE) or other types of Optimized Pulse Patterns (OPP).
- **DO-PWM**: Direct outputs. The direct access to the output state ('1' or '0') enables the implementation of software-modulated techniques such as Model Predictive Control (MPC). This also supports the use PWM outputs as standard digital outputs (possibly with dead time).
- **SS-PWM**: Sort-and-Select modulation and balancing (2 arms of up to 8 modules). This sub-system offers hardware-level support for the operation of Modular Multilevel Converters or similar topologies.
- **SB-PWM**: Sandbox. This FPGA area is left available for the implementation of fully-customized modulation techniques, while providing drivers for an easy-to-use access from the software level.

At the output, each of the 32 PWM signals can be directly propagated to the physical outputs (electrical or optical), or to go through a dead time generator.
This results in 32 PWM lanes. By default, lanes are also arranged into 16 pairs of adjacent lanes designated as channels. Within a channel, odd lanes are always low-side signals, while even lanes are always high-side. PWM lanes #0-31 are available from the electrical connectors, while only PWM lanes #0-15 are produced on the optical outputs.
Dead time is obtained by delaying the rising edge of each PWM signal within a given pair. This results in an equivalent propagation delay of half the dead time.

Channel	0	1	2	...	7	8	9	10	...	15
Lane	*0*	*2*	*4*	*...*	*14*	*16*	*18*	*20*	*...*	*30*
	1	*3*	*5*	*...*	*15*	*17*	*19*	*21*	*...*	*31*

Table 23. Designation of the PWM lanes and channels.

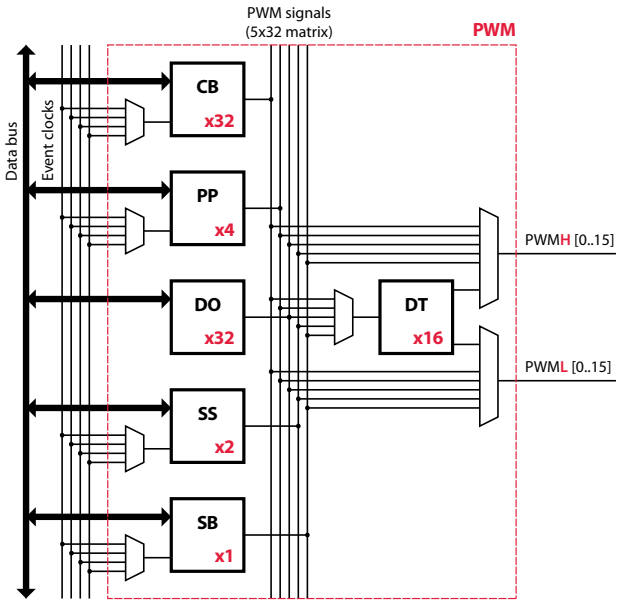


Fig. 14. Internal structure of the PWM signals generation block.

CB-PWM : CARRIER-BASED MODULATION

Carrier-based modulators offer the easiest way to generate pulse-width modulated signals. The corresponding subsystem features 32 independent modulators, which offer independent duty-cycle and phase parameters as well as four different types of carriers. With triangular carriers, modulators can be configured with single or double update rates (once or twice per PWM period).

Table 24.

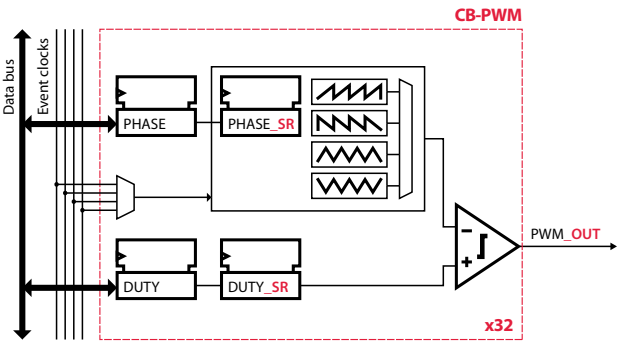


Fig. 15. Internal structure of the CB-PWM peripheral block.

Characteristic	Value
Counter depth	*16 bits*
Edge resolution (counter resolution)	*4 ns*

Table 25. Performance specifications of the CB-PWM block.

SV-PWM : SPACE VECTOR MODULATION

Space vector modulation (sometimes referred to as SVM) is supported through dedicated software drivers, making use of the same resources as the CB-PWM subsystem. Indeed, once the closed vectors have been identified and the suitable sequence determined, the switching events can be easily produced by suitably-programmed modulators.
SV-PWM automatically configures adjacent lanes or channels and supports single or double update rates.

DO-PWM : DIRECT OUTPUT ACCESS

Direct access to the PWM outputs is supported by the DO-PWM subsystem. It distinguishes from the SB-PWM in the sense that it is pre-implemented and requires no HDL editing. PWM state values (0 or 1) can be written directly from the CPU cores. This may typically be useful for model-predictive control (MPC) or sliding mode control techniques such as direct torque control (DTC).
Similarly to all PWM subsystems, when used as a channel, output lanes benefit from the dead-time generator block as well as protective mechanisms.

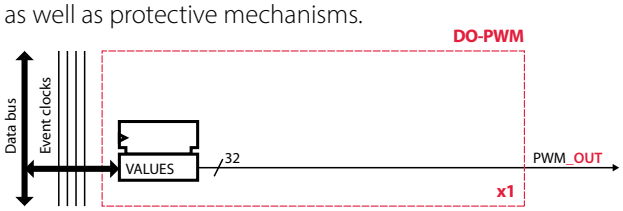


Fig. 16. Internal structure of the DO-PWM block.

SB-PWM : SANDBOX FOR OTHER TECHNIQUES

In addition to existing modulators, the B-Board also features a user-programmable area inside the FPGA . This notably allows implementing special own modulation techniques. In the sandbox, data read and write access from / to the CPU is provides from the the SBI and SBO blocks, respectively (see "User-programmable area (Sandbox)" on page 13).
The SB-PWM subsystem allows interfacing the PWM lanes through the dead-time generator block (see Fig. 19) as well as the B-Box's hardware protection mechanisms.

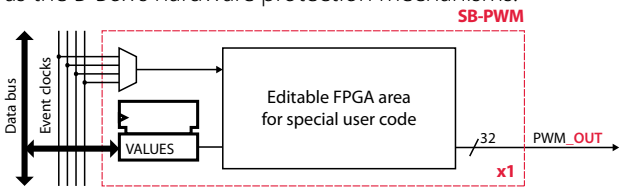


Fig. 17. Internal structure of the SB-PWM block.

PP-PWM : PROGRAMMED PATTERNS MODULATION

The programmed pattern blocks support modulation techniques that rely on pre-defined switching instants such as the generation of firing angles on a thyristor-based converter, the implementation of Selective Harmonic Elimination (SHE) or any Optimized Pulse Pattern (OPP). Three-phase system up to 3 levels are supported.
PP-PWM have a fixed counter period (hence angular resolution), but can nevertheless be fed by variable-frequency clocks (see CLK peripheral block), typically aiming to be integrated withing a software PLL.
Each PP-PWM block contains multiple look up tables (LUT) for switching angles, registers for indicating the direction (up or down) of each switching event, as well as an additional truth table for decoding the output state.
Obviously, the PP-PWM blocks are meant for accelerating the run time execution of OPP-based modulation and not for supporting the computation of the associated optimization algorithms.

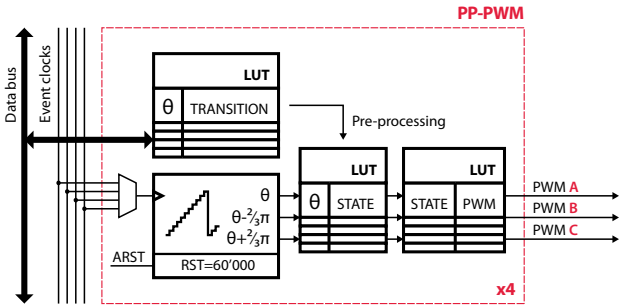


Fig. 18. Internal structure of the SS-PWM block.

Characteristic	Value
Number of angle registers (values 0 – 60'000)	*3x 16 angles x 16 bits*
Number of transition direction bits registers (up or down)	*3x 16 bits*
Edge resolution (respectively to signal period)	*0.017 ‰*

Table 26. Performance specifications of the PP-PWM block.

SS-PWM : SORT-AND-SELECT MODULATION FOR MODULAR MULTILEVEL CONVERTERS (MMC)

Modulation with integrated voltage balancing for multilevel converters is supported at the firmware level thanks to the SS-PWM block. It applies to Modular Multilevel Converters as well as similar topologies with floating submodules.
This subsystem accesses the voltages acquired on the analog inputs AIN 0-7 in order to sort the submodule voltages and allocate the switching events to the suitable submodule as a function of the current polarity (AIN 8 or 9).
The SS-PWM block is compatible with half- and full-bridge submodule topologies and hence with both positive and negative arm voltages. The pre-implemented solution also guarantees that only one submodule switches at a given time in order to minimize switching losses and optimize the ratio between apparent and actual switching frequencies.
Finally, the SS-PWM firmware also supports the exclusion of one or several submodules from the modulation process, as required by most fault-tolerant operation mechanisms.

Characteristic	Symbol	Value
Number or submodule per converter arm	*N*	*4, 8, 16 (–bypass)*
Number of output voltage levels	*L*	*N+1 or 2N+1*
Switching frequency range	f_{sw}	*3.72 Hz – 1 MHz*
PWM edge resolution		*40 ns*

Table 27. Performance specifications of the SS-PWM block.

DEAD TIME GENERATION SUBSYSTEM

As depicted by Fig. 14, the PWM block features a dead time generator at its output. This subsystem can be either used normally, or simply bypassed by picking-up the signals from the PWM matrix directly (outputs of the modulators).
Signals from all five PWM subsystems can be routed to the physical outputs (electrical only on B-Board).
The dead time generation relies on a finite state machine operating as depicted in Fig. 19. Essentially, the rising edges of the high-side and low-side signals are delayed by a programmable amount of time. This results in an equivalent propagation delay of half the dead time.
Intrinsically, this implementation guarantees that a signal pulse shorter than the dead time value is not produced.

Characteristic	Min.	Typ.	Max.	Unit
Dead time resolution		*4*		*ns*
Dead time value	*0.004*		*262*	*µs*

Table 28. Performance specifications of the dead time generation.

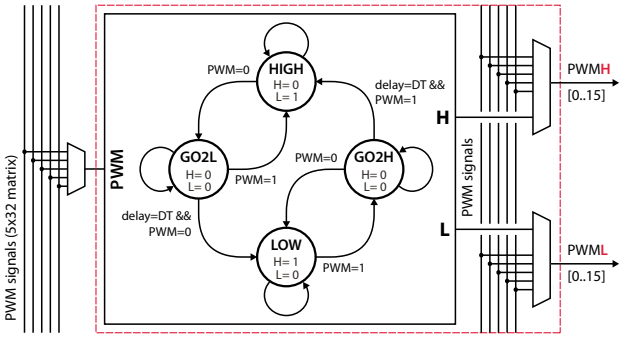


Fig. 19. Internal structure of the dead time generation block.

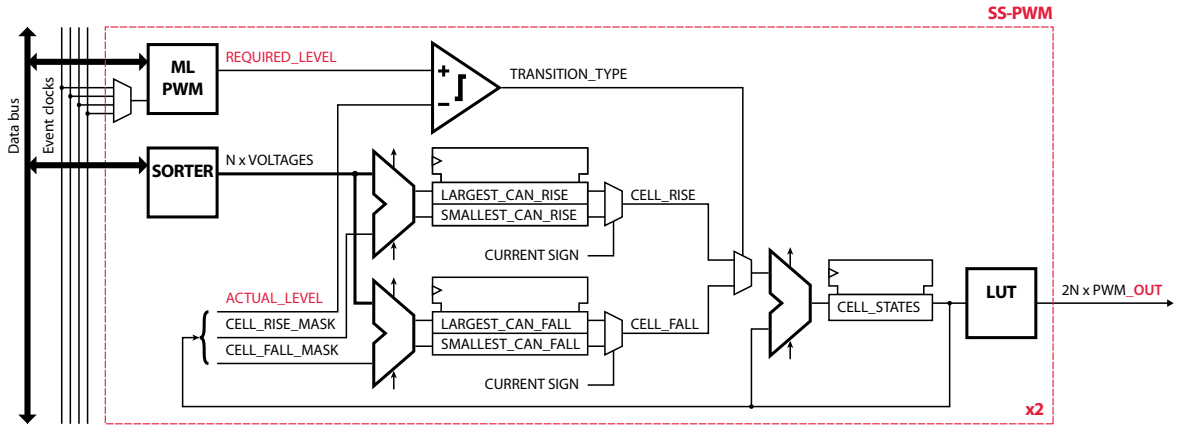


Fig. 24. Internal structure of the SS-PWM peripheral block.

DATA TRANSFER PERFORMANCE

The transfer of continuously-updated modulation parameters from the processing core to the distributed modulators causes delays, which depend on the amount of data to be transferred. Fig. 20 shows the achieved performance with respect to the update of the CB-PWM block. Other modulators perform similarly.

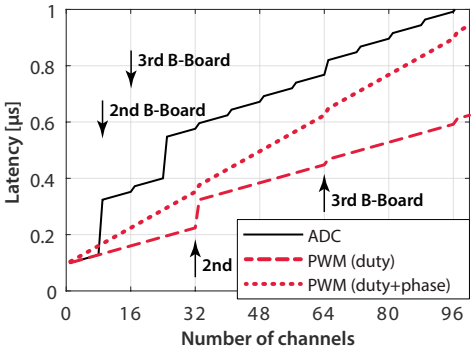


Fig. 20. Data transfer delay, as a function of the number of channels and number of B-Boards.

USER-PROGRAMMABLE AREA (SANDBOX)

The B-Board PRO is designed such that its FPGA area (PL) can embed user-defined programmable logic. This allows the implementation of special modulation techniques, proprietary communication mechanisms, or interfacing with external hardware.

Within this special area, designated as *sandbox*, two peripheral blocks are pre-implemented for easy-to-use I/O access from / to the CPU cores:

» SBI: Input from the sandbox
» SBO: Output to the sandbox

Also, the sandbox offers connectivity to the following I/O:

» ADC values (16x 16 bits signed integers)
» SB-PWM signals (32 bits register)
» Internal clocks
» Physical I/Os (FLT, USR, GPI, GPO)

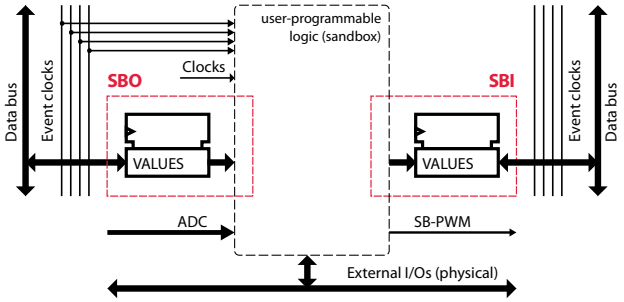


Fig. 21. Internal structure of the SBI and SBO blocks.

Thanks to the *RealSync* communication protocol, using the sandbox can be done the exact same way on a slave as on a master. Data transfers (read or write) from the CPU core are handled by the SBI or SBO blocks using either the write-through (configuration) or write-back (real-time) data traffic, as with any other peripheral block.

C/C++ drivers (as well as their blockset counterparts) are readily available in the software development kits (SDKs). On the programmable logic side, development templates are available on the web site or provided upon request. In the provided HDL source code, other peripheral blocks are obfuscated.

INCREMENTAL DECODERS

The B-Board features decoder inputs for quadrature-encoder speed / position sensor signals (usually called A and B), with or without a reset line (usually called Z). These inputs are either configurable as four independent sensor inputs or two differential inputs.

The decoder module counts all 4 edges of the A and B inputs, leading to an angular resolution 4 times better than the PPR value usually specified for a given encoder. Additionally, the position can be latched with a sampling, similar to the sample and hold feature of the ADC inputs.

Characteristic	Test conditions	Min.	Typ.	Max.	Unit
Input signals	*• Single-ended signaling: A, B and Z (Z is optional)* *• Differential signaling: A, $\overline{A}$, B, $\overline{B}$, Z, $\overline{Z}$ (Z, $\overline{Z}$ are optional)*				
Sampling options	*Either synchronized with ADC, or independent*				
PPR frequency	*Quadruple rate.*	*0*		*5*	*MHz*

Table 29. Performance specifications of the DEC block.

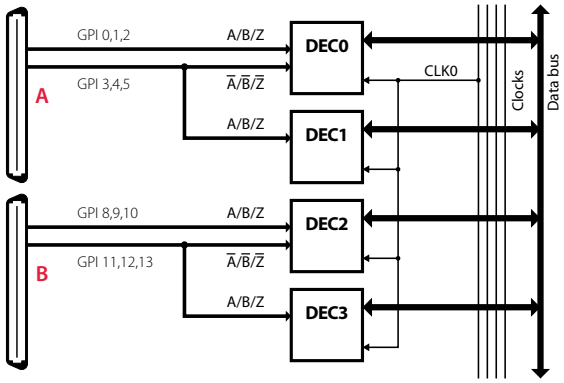


Fig. 22. Device mapping and configuration of the four incremental speed / position sensors decoders.

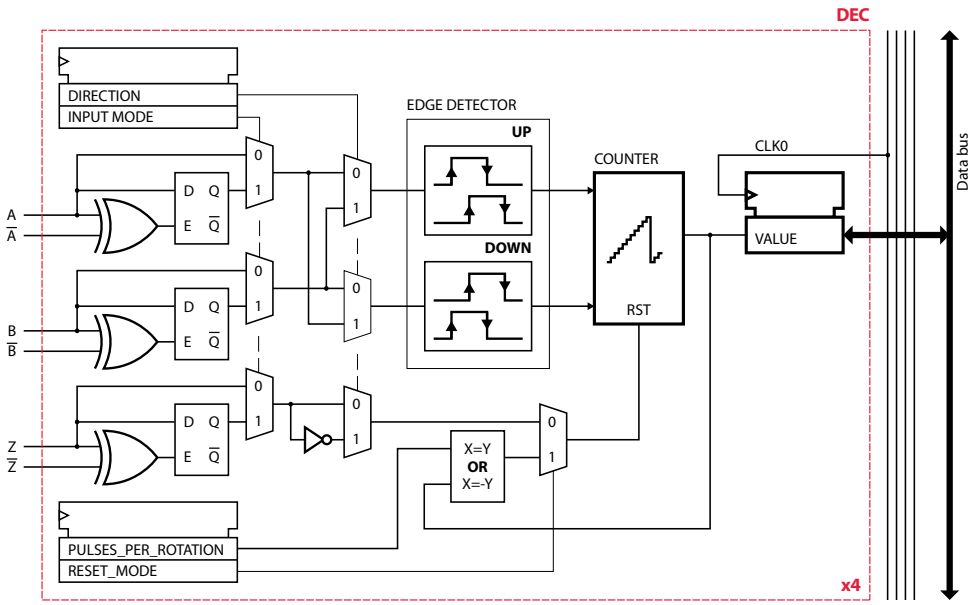


Fig. 23. Internal structure of the DEC block.

MECHANICAL DATA

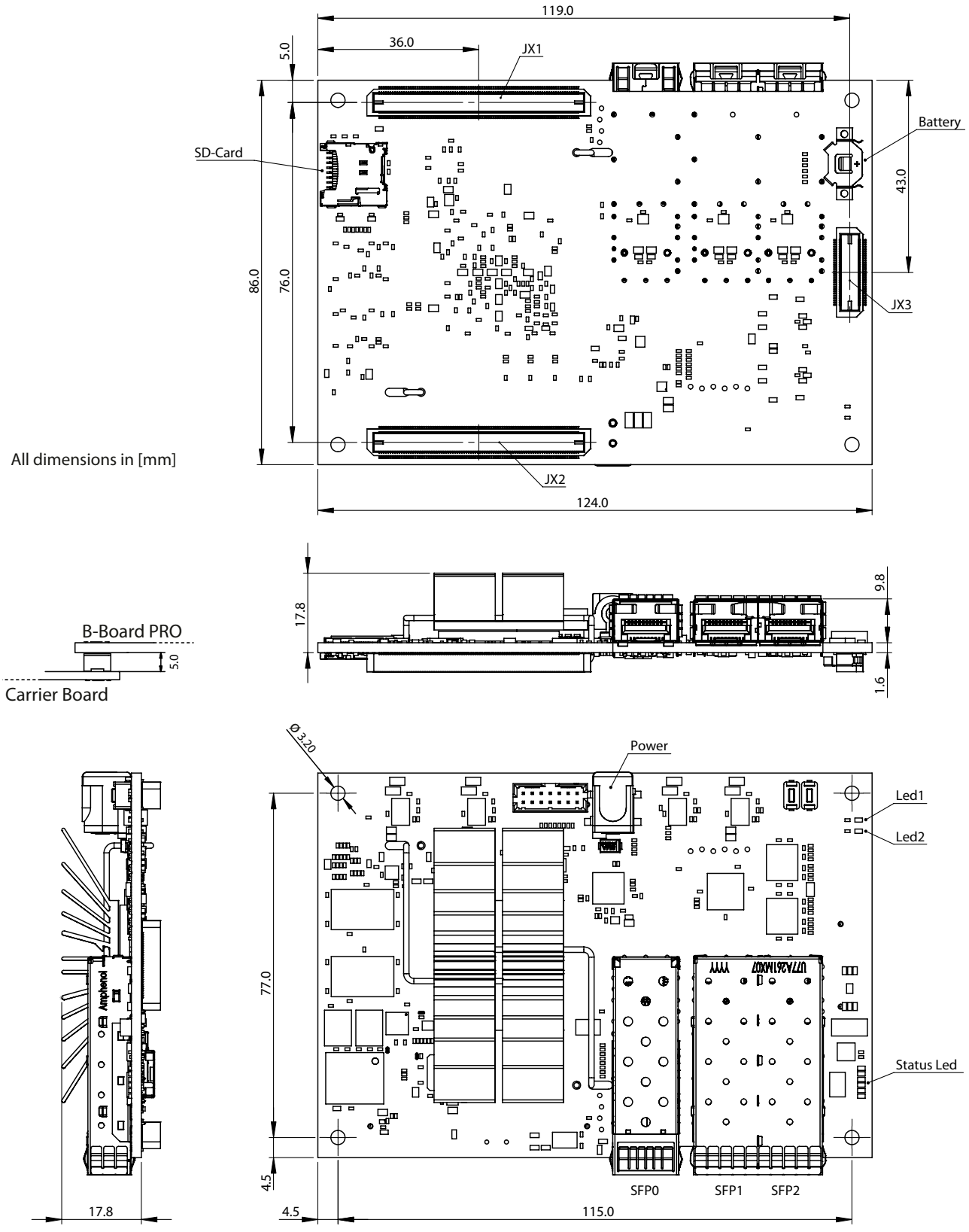


Fig. 25. Mechanical dimensions of B-Board PRO

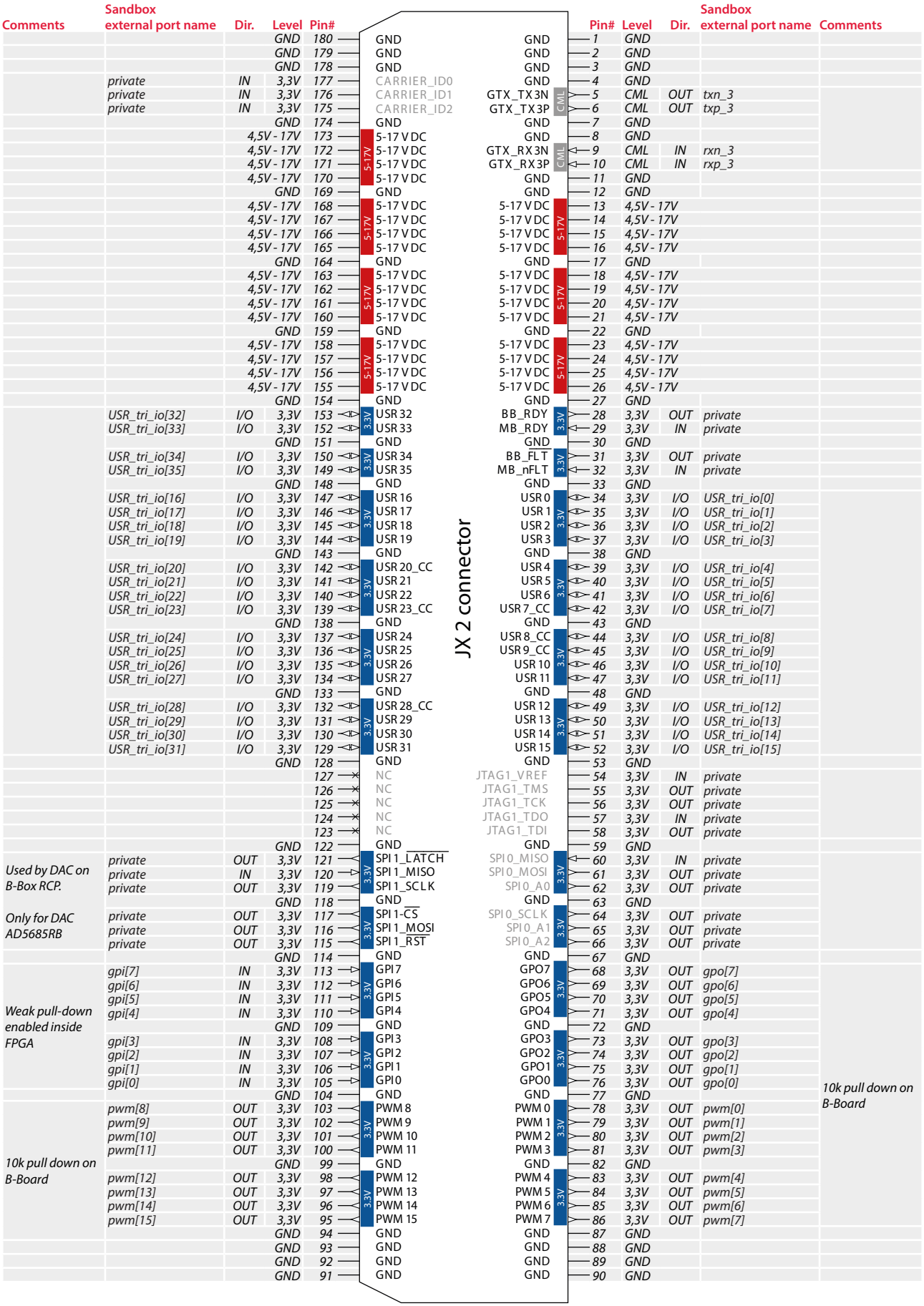
CONNECTOR JX1

Comments	Sandbox external port name	Dir.	Level	Pin#			Pin#	Level	Dir.	Sandbox external port name	Comments
			GND	90		GND	91	GND			
			GND	89		GND	92	GND			
			GND	88		GND	93	GND			
	gpi[15]	IN	3,3V	87	GPI15	GPO15	94	3,3V	OUT	gpo[15]	
	gpi[14]	IN	3,3V	86	GPI14	GPO14	95	3,3V	OUT	gpo[14]	
	gpi[13]	IN	3,3V	85	GPI13	GPO13	96	3,3V	OUT	gpo[13]	
Level-shifted from 3,3V to 1,8V on B-Board side	gpi[12]	IN	3,3V	84	GPI12	GPO12	97	3,3V	OUT	gpo[12]	Level-shifted from 1V8 to 3V3 on B-Board side
			GND	83	GND	GND	98	GND			
	gpi[11]	IN	3,3V	82	GPI11	GPO11	99	3,3V	OUT	gpo[11]	
	gpi[10]	IN	3,3V	81	GPI10	GPO10	100	3,3V	OUT	gpo[10]	
	gpi[9]	IN	3,3V	80	GPI9	GPO9	101	3,3V	OUT	gpo[9]	
	gpi[8]	IN	3,3V	79	GPI8	GPO8	102	3,3V	OUT	gpo[8]	
			GND	78	GND	GND	103	GND			
	flt[0]	IN	1,8V	77	1V8FLT0	1V8PWM 16	104	1,8V	OUT	pwm[16]	
	flt[1]	IN	1,8V	76	1V8FLT1	1V8PWM 17	105	1,8V	OUT	pwm[17]	
	flt[2]	IN	1,8V	75	1V8FLT2	1V8PWM 18	106	1,8V	OUT	pwm[18]	
	flt[3]	IN	1,8V	74	1V8FLT3	1V8PWM 19	107	1,8V	OUT	pwm[19]	
			GND	73	GND	GND	108	GND			
	flt[4]	IN	1,8V	72	1V8FLT4	1V8PWM 20	109	1,8V	OUT	pwm[20]	
	flt[5]	IN	1,8V	71	1V8FLT5	1V8PWM 21	110	1,8V	OUT	pwm[21]	
	flt[6]	IN	1,8V	70	1V8FLT6	1V8PWM 22	111	1,8V	OUT	pwm[22]	
Weak pull-down enabled inside FPGA	flt[7]	IN	1,8V	69	1V8FLT7	1V8PWM 23	112	1,8V	OUT	pwm[23]	10k pull down on B-Board
			GND	68	GND	GND	113	GND			
	flt[8]	IN	1,8V	67	1V8FLT8	1V8PWM 24	114	1,8V	OUT	pwm[24]	
	flt[9]	IN	1,8V	66	1V8FLT9	1V8PWM 25	115	1,8V	OUT	pwm[25]	
	flt[10]	IN	1,8V	65	1V8FLT10	1V8PWM 26	116	1,8V	OUT	pwm[26]	
	flt[11]	IN	1,8V	64	1V8FLT11	1V8PWM 27	117	1,8V	OUT	pwm[27]	
			GND	63	GND	GND	118	GND			
	flt[12]	IN	1,8V	62	1V8FLT12	1V8PWM 28	119	1,8V	OUT	pwm[28]	
	flt[13]	IN	1,8V	61	1V8FLT13	1V8PWM 29	120	1,8V	OUT	pwm[29]	
	flt[14]	IN	1,8V	60	1V8FLT14	1V8PWM 30	121	1,8V	OUT	pwm[30]	
	flt[15]	IN	1,8V	59	1V8FLT15	1V8PWM 31	122	1,8V	OUT	pwm[31]	
			GND	58	GND	GND	123	GND			
	vhdca[0]	I/O	1,8V	57	1V8VHDCA0	1V8BBOX44	124	1,8V	I/O	BBOX_tri_io[44]	
	vhdca[1]	I/O	1,8V	56	1V8VHDCA1	1V8BBOX45	125	1,8V	I/O	BBOX_tri_io[45]	
	vhdca[2]	I/O	1,8V	55	1V8VHDCA2	1V8BBOX46	126	1,8V	I/O	BBOX_tri_io[46]	
	vhdca[3]	I/O	1,8V	54	1V8VHDCA3	1V8BBOX47	127	1,8V	I/O	BBOX_tri_io[47]	
			GND	53	GND	GND	128	GND			
	BBOX_tri_io[50]	I/O	1,8V	52	1V8BBOX50	1V8BBOX48	129	1,8V	I/O	BBOX_tri_io[48]	
	BBOX_tri_io[51]	I/O	1,8V	51	1V8BBOX51	1V8BBOX49	130	1,8V	I/O	BBOX_tri_io[49]	
			GND	50	GND	GND	131	GND			
	BBOX_tri_io[0]	I/O	1,8V	49	1V8BBOX0	1V8BBOX22	132	1,8V	I/O	BBOX_tri_io[22]	
	BBOX_tri_io[1]	I/O	1,8V	48	1V8BBOX1	1V8BBOX23	133	1,8V	I/O	BBOX_tri_io[23]	
			GND	47	GND	GND	134	GND			
	BBOX_tri_io[2]	I/O	1,8V	46	1V8BBOX2	1V8BBOX24	135	1,8V	I/O	BBOX_tri_io[24]	
	BBOX_tri_io[3]	I/O	1,8V	45	1V8BBOX3	1V8BBOX25	136	1,8V	I/O	BBOX_tri_io[25]	
			GND	44	GND	GND	137	GND			
	BBOX_tri_io[4]	I/O	1,8V	43	1V8BBOX4_CC	1V8BBOX26	138	1,8V	I/O	BBOX_tri_io[26]	
	BBOX_tri_io[5]	I/O	1,8V	42	1V8BBOX5	1V8BBOX27	139	1,8V	I/O	BBOX_tri_io[27]	Used by imperix B-Box RCP
			GND	41	GND	GND	140	GND			
Used by imperix B-Box RCP	BBOX_tri_io[6]	I/O	1,8V	40	1V8BBOX6	1V8BBOX28	141	1,8V	I/O	BBOX_tri_io[28]	
	BBOX_tri_io[7]	I/O	1,8V	39	1V8BBOX7	1V8BBOX29	142	1,8V	I/O	BBOX_tri_io[29]	Pins avaible only for custom carrier board design
	BBOX_tri_io[8]	I/O	1,8V	38	1V8BBOX8	1V8BBOX30	143	1,8V	I/O	BBOX_tri_io[30]	
Pins avaible only for custom carrier board design	BBOX_tri_io[9]	I/O	1,8V	37	1V8BBOX9	1V8BBOX31	144	1,8V	I/O	BBOX_tri_io[31]	
			GND	36	GND	GND	145	GND			
	BBOX_tri_io[10]	I/O	1,8V	35	1V8BBOX10	1V8BBOX32	146	1,8V	I/O	BBOX_tri_io[32]	
	BBOX_tri_io[11]	I/O	1,8V	34	1V8BBOX11	1V8BBOX33	147	1,8V	I/O	BBOX_tri_io[33]	
	BBOX_tri_io[12]	I/O	1,8V	33	1V8BBOX12	1V8BBOX34	148	1,8V	I/O	BBOX_tri_io[34]	
	BBOX_tri_io[13]	I/O	1,8V	32	1V8BBOX13	1V8BBOX35	149	1,8V	I/O	BBOX_tri_io[35]	
			GND	31	GND	GND	150	GND			
	BBOX_tri_io[14]	I/O	1,8V	30	1V8BBOX14	1V8BBOX36	151	1,8V	I/O	BBOX_tri_io[36]	
	BBOX_tri_io[15]	I/O	1,8V	29	1V8BBOX15_CC	1V8BBOX37	152	1,8V	I/O	BBOX_tri_io[37]	
	BBOX_tri_io[16]	I/O	1,8V	28	1V8BBOX16	1V8BBOX38	153	1,8V	I/O	BBOX_tri_io[38]	
	BBOX_tri_io[17]	I/O	1,8V	27	1V8BBOX17	1V8BBOX39	154	1,8V	I/O	BBOX_tri_io[39]	
			GND	26	GND	GND	155	GND			
	BBOX_tri_io[18]	I/O	1,8V	25	1V8BBOX18_CC	1V8BBOX40	156	1,8V	I/O	BBOX_tri_io[40]	
	BBOX_tri_io[19]	I/O	1,8V	24	1V8BBOX19	1V8BBOX41_CC	157	1,8V	I/O	BBOX_tri_io[41]	
	BBOX_tri_io[20]	I/O	1,8V	23	1V8BBOX20	1V8BBOX42	158	1,8V	I/O	BBOX_tri_io[42]	
	BBOX_tri_io[21]	I/O	1,8V	22	1V8BBOX21	1V8BBOX43	159	1,8V	I/O	BBOX_tri_io[43]	
			GND	21	GND	GND	160	GND			
				20	PHY_MDI0_P	NC	161				
				19	PHY_MDI0_N	NC	162				
			GND	18	GND	GND	163	GND			
				17	PHY_MDI1_P	NC	164				
				16	PHY_MDI1_N	NC	165				
			GND	15	GND	GND	166	GND			
				14	PHY_MDI2_P	PHY_LED0	167				
Ethernet Interface				13	PHY_MDI2_N	PHY_LED1	168				
			GND	12	GND	GND	169	GND			
				11	PHY_MDI3_P	OTG_VBUS	170				
				10	PHY_MDI3_N	OTG_VBUS	171				
			GND	9	GND	GND	172	GND			
				8	OTG_D_N	NC	173				
				7	OTG_D_P	NC	174				
			GND	6	GND	GND	175	GND			
				5	OTG_ID	CAN_TX	176				
				4	OTG_CPEN	CAN_RX	177				
			GND	3	GND	GND	178	GND			
			GND	2	GND	GND	179	GND			
			GND	1	GND	GND	180	GND			

JX 1 connector

- Gray pins should not be used and connected !
- The _CC suffix on the pins indicates that the signal can be used as a clock input

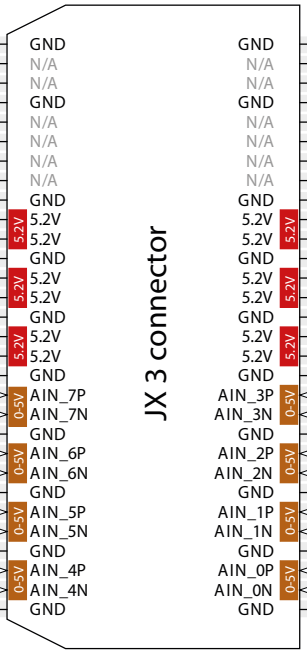
CONNECTOR JX2



Comments	Sandbox external port name	Dir.	Level	Pin#			Pin#	Level	Dir.	Sandbox external port name	Comments
			GND	180	GND	GND	1	GND			
			GND	179	GND	GND	2	GND			
			GND	178	GND	GND	3	GND			
	private	IN	3,3V	177	CARRIER_ID0	GND	4	GND			
	private	IN	3,3V	176	CARRIER_ID1	GTX_TX3N	5	CML	OUT	txn_3	
	private	IN	3,3V	175	CARRIER_ID2	GTX_TX3P	6	CML	OUT	txp_3	
			GND	174	GND	GND	7	GND			
			4,5V - 17V	173	5-17 V DC	GND	8	GND			
			4,5V - 17V	172	5-17 V DC	GTX_RX3N	9	CML	IN	rxn_3	
			4,5V - 17V	171	5-17 V DC	GTX_RX3P	10	CML	IN	rxp_3	
			4,5V - 17V	170	5-17 V DC	GND	11	GND			
			GND	169	GND	GND	12	GND			
			4,5V - 17V	168	5-17 V DC	5-17 V DC	13	4,5V - 17V			
			4,5V - 17V	167	5-17 V DC	5-17 V DC	14	4,5V - 17V			
			4,5V - 17V	166	5-17 V DC	5-17 V DC	15	4,5V - 17V			
			4,5V - 17V	165	5-17 V DC	5-17 V DC	16	4,5V - 17V			
			GND	164	GND	GND	17	GND			
			4,5V - 17V	163	5-17 V DC	5-17 V DC	18	4,5V - 17V			
			4,5V - 17V	162	5-17 V DC	5-17 V DC	19	4,5V - 17V			
			4,5V - 17V	161	5-17 V DC	5-17 V DC	20	4,5V - 17V			
			4,5V - 17V	160	5-17 V DC	5-17 V DC	21	4,5V - 17V			
			GND	159	GND	GND	22	GND			
			4,5V - 17V	158	5-17 V DC	5-17 V DC	23	4,5V - 17V			
			4,5V - 17V	157	5-17 V DC	5-17 V DC	24	4,5V - 17V			
			4,5V - 17V	156	5-17 V DC	5-17 V DC	25	4,5V - 17V			
			4,5V - 17V	155	5-17 V DC	5-17 V DC	26	4,5V - 17V			
			GND	154	GND	GND	27	GND			
	USR_tri_io[32]	I/O	3,3V	153	USR 32	BB_RDY	28	3,3V	OUT	private	
	USR_tri_io[33]	I/O	3,3V	152	USR 33	MB_RDY	29	3,3V	IN	private	
			GND	151	GND	GND	30	GND			
	USR_tri_io[34]	I/O	3,3V	150	USR 34	BB_FLT	31	3,3V	OUT	private	
	USR_tri_io[35]	I/O	3,3V	149	USR 35	MB_nFLT	32	3,3V	IN	private	
			GND	148	GND	GND	33	GND			
	USR_tri_io[16]	I/O	3,3V	147	USR 16	USR 0	34	3,3V	I/O	USR_tri_io[0]	
	USR_tri_io[17]	I/O	3,3V	146	USR 17	USR 1	35	3,3V	I/O	USR_tri_io[1]	
	USR_tri_io[18]	I/O	3,3V	145	USR 18	USR 2	36	3,3V	I/O	USR_tri_io[2]	
	USR_tri_io[19]	I/O	3,3V	144	USR 19	USR 3	37	3,3V	I/O	USR_tri_io[3]	
			GND	143	GND	GND	38	GND			
	USR_tri_io[20]	I/O	3,3V	142	USR 20_CC	USR 4	39	3,3V	I/O	USR_tri_io[4]	
	USR_tri_io[21]	I/O	3,3V	141	USR 21	USR 5	40	3,3V	I/O	USR_tri_io[5]	
	USR_tri_io[22]	I/O	3,3V	140	USR 22	USR 6	41	3,3V	I/O	USR_tri_io[6]	
	USR_tri_io[23]	I/O	3,3V	139	USR 23_CC	USR 7_CC	42	3,3V	I/O	USR_tri_io[7]	
			GND	138	GND	GND	43	GND			
	USR_tri_io[24]	I/O	3,3V	137	USR 24	USR 8_CC	44	3,3V	I/O	USR_tri_io[8]	
	USR_tri_io[25]	I/O	3,3V	136	USR 25	USR 9_CC	45	3,3V	I/O	USR_tri_io[9]	
	USR_tri_io[26]	I/O	3,3V	135	USR 26	USR 10	46	3,3V	I/O	USR_tri_io[10]	
	USR_tri_io[27]	I/O	3,3V	134	USR 27	USR 11	47	3,3V	I/O	USR_tri_io[11]	
			GND	133	GND	GND	48	GND			
	USR_tri_io[28]	I/O	3,3V	132	USR 28_CC	USR 12	49	3,3V	I/O	USR_tri_io[12]	
	USR_tri_io[29]	I/O	3,3V	131	USR 29	USR 13	50	3,3V	I/O	USR_tri_io[13]	
	USR_tri_io[30]	I/O	3,3V	130	USR 30	USR 14	51	3,3V	I/O	USR_tri_io[14]	
	USR_tri_io[31]	I/O	3,3V	129	USR 31	USR 15	52	3,3V	I/O	USR_tri_io[15]	
			GND	128	GND	GND	53	GND			
				127	NC	JTAG1_VREF	54	3,3V	IN	private	
				126	NC	JTAG1_TMS	55	3,3V	OUT	private	
				125	NC	JTAG1_TCK	56	3,3V	OUT	private	
				124	NC	JTAG1_TDO	57	3,3V	IN	private	
				123	NC	JTAG1_TDI	58	3,3V	OUT	private	
			GND	122	GND	GND	59	GND			
	private	OUT	3,3V	121	SPI 1_LATCH	SPI0_MISO	60	3,3V	IN	private	
Used by DAC on B-Box RCP.	private	IN	3,3V	120	SPI 1_MISO	SPI0_MOSI	61	3,3V	OUT	private	
	private	OUT	3,3V	119	SPI 1_SCLK	SPI0_A0	62	3,3V	OUT	private	
			GND	118	GND	GND	63	GND			
Only for DAC AD5685RB	private	OUT	3,3V	117	SPI 1-CS	SPI0_SCLK	64	3,3V	OUT	private	
	private	OUT	3,3V	116	SPI 1_MOSI	SPI0_A1	65	3,3V	OUT	private	
	private	OUT	3,3V	115	SPI 1_RST	SPI0_A2	66	3,3V	OUT	private	
			GND	114	GND	GND	67	GND			
	gpi[7]	IN	3,3V	113	GPI7	GPO7	68	3,3V	OUT	gpo[7]	
	gpi[6]	IN	3,3V	112	GPI6	GPO6	69	3,3V	OUT	gpo[6]	
	gpi[5]	IN	3,3V	111	GPI5	GPO5	70	3,3V	OUT	gpo[5]	
Weak pull-down enabled inside FPGA	gpi[4]	IN	3,3V	110	GPI4	GPO4	71	3,3V	OUT	gpo[4]	
			GND	109	GND	GND	72	GND			
	gpi[3]	IN	3,3V	108	GPI3	GPO3	73	3,3V	OUT	gpo[3]	
	gpi[2]	IN	3,3V	107	GPI2	GPO2	74	3,3V	OUT	gpo[2]	
	gpi[1]	IN	3,3V	106	GPI1	GPO1	75	3,3V	OUT	gpo[1]	
	gpi[0]	IN	3,3V	105	GPI0	GPO0	76	3,3V	OUT	gpo[0]	
			GND	104	GND	GND	77	GND			10k pull down on B-Board
	pwm[8]	OUT	3,3V	103	PWM 8	PWM 0	78	3,3V	OUT	pwm[0]	
	pwm[9]	OUT	3,3V	102	PWM 9	PWM 1	79	3,3V	OUT	pwm[1]	
	pwm[10]	OUT	3,3V	101	PWM 10	PWM 2	80	3,3V	OUT	pwm[2]	
	pwm[11]	OUT	3,3V	100	PWM 11	PWM 3	81	3,3V	OUT	pwm[3]	
10k pull down on B-Board			GND	99	GND	GND	82	GND			
	pwm[12]	OUT	3,3V	98	PWM 12	PWM 4	83	3,3V	OUT	pwm[4]	
	pwm[13]	OUT	3,3V	97	PWM 13	PWM 5	84	3,3V	OUT	pwm[5]	
	pwm[14]	OUT	3,3V	96	PWM 14	PWM 6	85	3,3V	OUT	pwm[6]	
	pwm[15]	OUT	3,3V	95	PWM 15	PWM 7	86	3,3V	OUT	pwm[7]	
			GND	94	GND	GND	87	GND			
			GND	93	GND	GND	88	GND			
			GND	92	GND	GND	89	GND			
			GND	91	GND	GND	90	GND			

CONNECTOR JX3

Comments	Sandbox external port name	Dir.	Level	Pin#			Pin#	Level	Dir.	Sandbox external port name	Comments
			GND	60	GND	GND	1	GND			
				59	N/A	N/A	2				
				58	N/A	N/A	3				
			GND	57	GND	GND	4	GND			
				56	N/A	N/A	5				
				55	N/A	N/A	6				
				54	N/A	N/A	7				
				53	N/A	N/A	8				
			GND	52	GND	GND	9	GND			
			5,2V	51	5.2V	5.2V	10	5,2V			
			5,2V	50	5.2V	5.2V	11	5,2V			
			GND	49	GND	GND	12	GND			
			5,2V	48	5.2V	5.2V	13	5,2V			
			5,2V	47	5.2V	5.2V	14	5,2V			
			GND	46	GND	GND	15	GND			
			5,2V	45	5.2V	5.2V	16	5,2V			
			5,2V	44	5.2V	5.2V	17	5,2V			
			GND	43	GND	GND	18	GND			
		IN	0-5V	42	AIN_7P	AIN_3P	19	0-5V	IN		
		IN	0-5V	41	AIN_7N	AIN_3N	20	0-5V	IN		
			GND	40	GND	GND	21	GND			
		IN	0-5V	39	AIN_6P	AIN_2P	22	0-5V	IN		
		IN	0-5V	38	AIN_6N	AIN_2N	23	0-5V	IN		
			GND	37	GND	GND	24	GND			
		IN	0-5V	36	AIN_5P	AIN_1P	25	0-5V	IN		
		IN	0-5V	35	AIN_5N	AIN_1N	26	0-5V	IN		
			GND	34	GND	GND	27	GND			
		IN	0-5V	33	AIN_4P	AIN_0P	28	0-5V	IN		
		IN	0-5V	32	AIN_4N	AIN_0N	29	0-5V	IN		
			GND	31	GND	GND	30	GND			



REVISION HISTORY

- 14.01.20 : Initial release
- 10.02.20 : Additional details regarding the SBI, SBO and SB-PWM blocks.
- 20.04.20 : Clarification on ADC inputs.
- 05.02.24 : Modified pinout description
- 07.06.24 : Booting sequence table

This product must be used in electric / electronic equipment with respect to applicable standards and safety requirements in accordance with the manufacturer's operating instructions.
Caution, risk of electrical shock! When using the devices, certain parts of the modules may carry hazardous voltages (e.g. power supplies, busbars, etc.). Disregarding this warning may lead to injury and / or cause serious damage. All conducting parts must be inaccessible after installation.

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ABOUT US

Imperix Ltd is a company established in Sion, Switzerland. Its name is derived form the Latin verb imperare, which stands for controlling and refers to the company's core business: the control of power electronic systems. Imperix commercializes hardware and software solutions related to the fast and secure implementation of pilot systems and plants in the field of power conversion, energy storage and smart grids.

NOTE

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Data may change, as well as legislation, and the reader is strongly advised to obtain copies of the most recently issued regulations, standards, and guidelines.