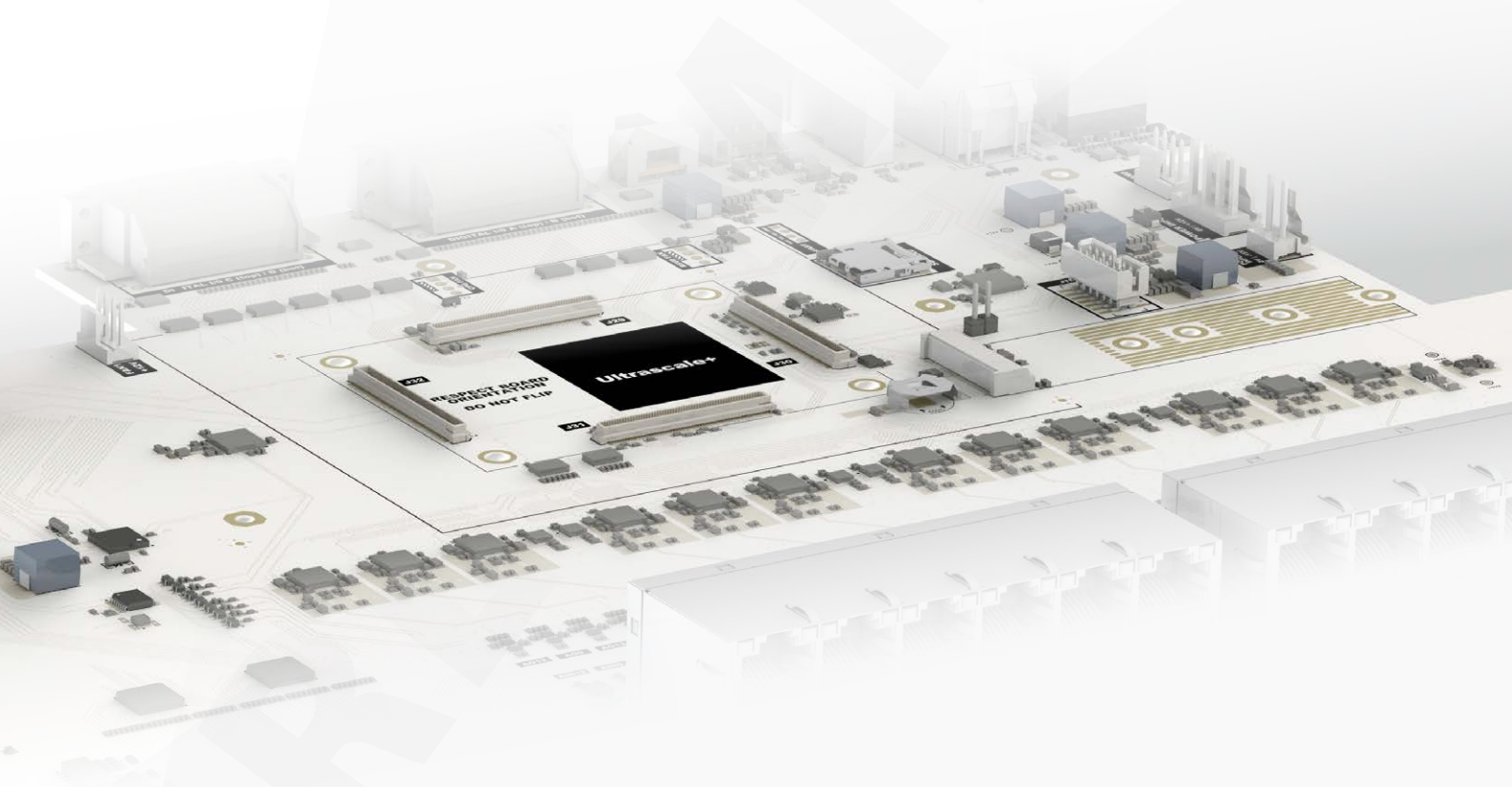




## B-BOX 4

ADVANCED PROTOTYPING CONTROLLER



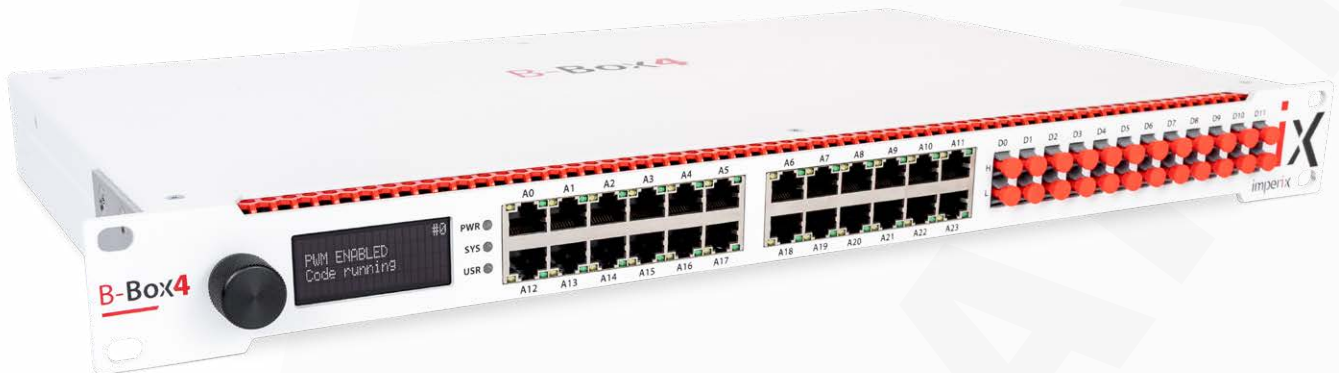
HIGH-PERFORMANCE SOLUTIONS FOR  
CONTROL DEVELOPMENT AND TESTING

imperix

“Certainly the most advanced rapid control prototyping solution for power electronics.”

# B-BOX 4

## ADVANCED PROTOTYPING CONTROLLER



### GENERAL DESCRIPTION

The B-Box 4 is imperix's flagship system for rapid control prototyping. It is a flexible, high-performance, and user-friendly programmable digital controller, designed to facilitate and accelerate the experimental validation of control algorithms in power electronics.

Designed with advanced control applications in mind, this **4th-generation controller** uses high-performance peripherals, making it ready for today's demanding needs as well as tomorrow's upcoming challenges. Simultaneously, the controller is also highly resourceful for conventional applications, thanks to the easy and rapid programming possibilities that already contributed to its predecessor's success.

The most unique feature of the B-Box 4 is certainly its analog acquisition stage, offering **24 channels** operating at rates up to **20 Msps**, supported by robust, low-noise, high-CMRR analog inputs, featuring over **2.5MHz** of bandwidth.

At its heart, the B-Box 4 is equipped with a quad-core 1.5GHz CPU with direct low-latency access to a AMD **Kintex FPGA**. These resources, effectively leveraged by a highly-optimized bare-metal implementation, enable control frequencies up to **500kHz**.

The controller further integrates six pre-implemented pulse-width modulator types, including **20-bit** carrier-based PWMs with an outstanding resolution of **250ps**.

For large applications with extended I/O requirements, up to **64 units** can be stacked using **40Gbps** optical links. Instant scalability is guaranteed by imperix's RealSync technology, offering precise synchronization and ultra low latency communication throughout the control network.

Finally, as with other imperix controllers, the B-Box 4's **FPGA** is accessible to its users, allowing them to freely edit part of the firmware for maximum flexibility and upgradability.

### KEY SPECIFICATIONS

| Component                            | Remarks                                                                 | B-Box RCP 3.0                                                       | B-Box 4 (this product)                                                  | Increase      |
|--------------------------------------|-------------------------------------------------------------------------|---------------------------------------------------------------------|-------------------------------------------------------------------------|---------------|
| Processing system                    | Now AMD Zynq Ultrascale+ 7EV, the largest FPGA supported by Vivado free | 2x 1.0GHz AMD Cortex A9 -3<br>1GB DDR3<br>8GB eMMC<br>Kintex 7 125K | 4x 1.5GHz AMD Cortex A53 -3<br>8GB DDR4<br>500GB SSD<br>Kintex US+ 504K | +50-80%<br>x4 |
| Analog inputs                        | Now bidirectional channels<br>Now with significantly larger bandwidth   | 16x 16bits 500ksps<br>400kHz analog bandwidth                       | 24x 16bits 20Msps<br>2.7MHz analog bandwidth                            | x40<br>x6     |
| Analog outputs                       |                                                                         | 4x 16bits 100ksps                                                   | 24x 12bits 500ksps                                                      |               |
| PWM outputs                          | Including support for CM-PWM, SV-PWM, SS-PWM, PP-PWM, DO-PWM and SB-PWM | 32x lanes / 16x channels<br>4ns resolution                          | 48x lanes / 24x channels<br>250ps resolution                            | +50%          |
| Multi-devices stacking               | Operating using Imperix RealSync                                        | 3x 10Gbps SFP+                                                      | 4x 40Gbps QSFP+                                                         | x5            |
| CAN                                  |                                                                         | 1x CAN (standard)                                                   | 2x CAN 2.0B/ CAN-FD                                                     |               |
| RS485 / RS422                        | Now with support for BiSS-C / SSI / EnDat 2.2                           | -                                                                   | 2x TX+ 2x RX/TX                                                         |               |
| General-purpose inputs (GPI)         | Now shared with FLT inputs                                              | 16x                                                                 | 24x                                                                     |               |
| General-purpose outputs (GPO)        | Now shared with PWM outputs                                             | 16x                                                                 | 24x                                                                     |               |
| Bidirectional direct FPGA I/Os (USR) | Straight from/to the FPGA                                               | 36x                                                                 | 36x                                                                     |               |
| Interlock                            | Fault coordination with 3-party devices                                 | 1x                                                                  | 1x                                                                      |               |

Table 1. Key specifications of the B-Box 4, compared to the previous generation.

## FRONT VIEW

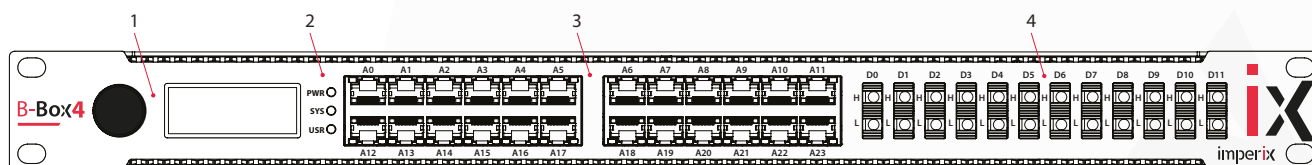


Fig. 1. Front panel view of the B-Box 4.

1. Front panel (rotary button and OLED screen)
2. Power, system, and user LEDs
3. Analog I/O channels (RJ45,  $\pm 10V$ )
4. Optical PWM outputs (first 24 lanes)

## REAR VIEW

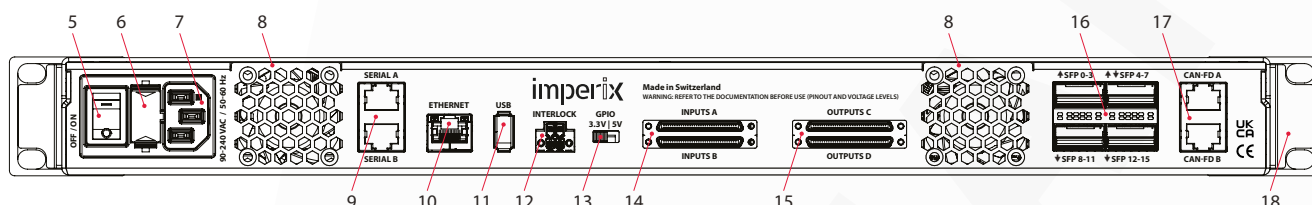


Fig. 2. Back panel view of the B-Box 4.

5. AC mains switch (ON/OFF)
6. AC mains fuse (1.0 A)
7. AC mains socket (IEC C14, 110-230V)
8. Cooling outlets
9. Serial ports (for SSI/BISS-C/EnDat)
10. Gigabit Ethernet (RJ45)
11. USB 3.0 socket (also compatible with USB 2.0)
12. Interlock connector (IN/OUT)
13. Selector for GPI/GPO/FLT/PWM voltage (3.3V or 5.0V)
14. Digital inputs – Connectors A and B
15. Digital outputs – Connectors C and D
16. QSFP+ sockets
17. Dual CAN-FD sockets (RJ45)
18. Reinforcement rack-mounting flanges

## HARDWARE ARCHITECTURE

The B-Box 4 is built around an AMD Zynq Ultrascale+, which directly provides most of the processing and I/O functions.

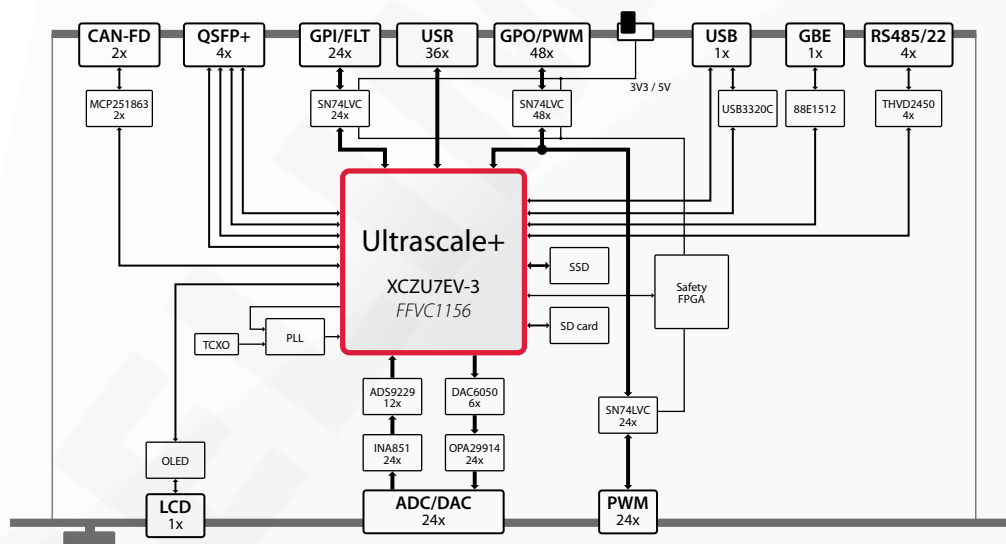


Fig. 3. Simplified internal architecture of the B-Box 4.

## SOFTWARE ARCHITECTURE

For optimum performance, software execution is distributed across several CPU cores as well as FPGA-based resources: The architecture is as follows:

- **CPU0+CPU1**: Based on embedded Linux, these cores are responsible for loading and supervising the user application (on CPU2), running the data logging, etc. These cores are not user-programmable.
- **CPU2**: Based on imperix's bare-metal kernel, this core executes the user-developed application-level control code as a hard real-time periodic routine.
- **FPGA**: The programmable logic (PL) inside the Ultrascale+ contains the application-specific peripherals. This encompasses the mandatory logic (imperix IP core) as well as the optional user logic inside the so-called sandbox.

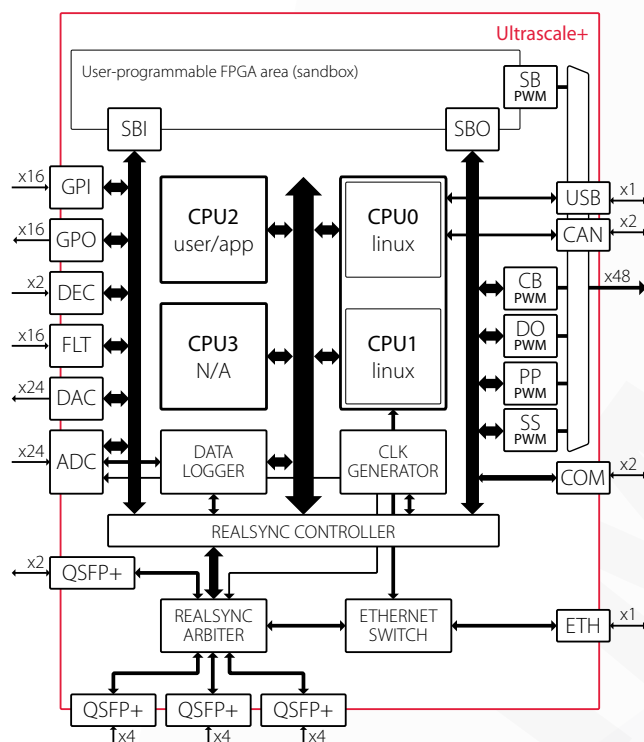


Fig. 4. Functional overview of the B-Box 4 controller.

## CONNECTIVITY

### ETHERNET

The Ethernet interface enables communication with the PC for both B-Box 4 programming (e.g., from Simulink or PLECS) and for live operational control using Imperix Cockpit. The same Ethernet link simultaneously supports exchanges from/to the user application using **UDP** and **Modbus TCP**. Furthermore, remote management is possible over **OPC-UA**.

### CAN

Data exchanges from/to the user application can be implemented thanks to two separate CAN busses with flexible data rate (-FD) and up to 29-bit identifiers (CAN 2.0B).

### RS485 / RS422

Two separate sockets with TX+RX/TX I/O streams implement RS485 / RS422-like communication for digital encoders. The supported protocols are **SSI**, **BiSS-C** and **EnDat 2.0**.

The pre-implemented FPGA peripherals are as follows:

- **CLK**: Offers up to four clock generators with separate time bases can be used within other peripherals.
- **ADC**: Acquires data from all 24 analog I/O channels.
- **DAC**: Updates the analog I/O channels that are configured as outputs.
- **SBI**: Provides easy-to-use inbound data traffic from the user-programmable area (read registers from sandbox).
- **SBO**: Provides easy-to-use outbound data traffic from the user-programmable area (write registers to sandbox).
- **CB-PWM**: Contains 48 high-resolution carrier-based modulators with configurable phase and duty-cycle.
- **SS-PWM**: Implements multilevel modulation for modular converters using sort-&-select voltage balancing, such as commonly used in Modular Multilevel Converters (MMC).
- **PP-PWM**: Implements support for the generation of programmed patterns, such as Selective Harmonic Elimination (SHE) or Optimized Pulse Patterns (OPP).
- **DO-PWM**: Offers a direct output mode, allowing to force a specific lane state (0 or 1) directly from the CPU. This is useful for control techniques such as Model Predictive Control (MPC) or Direct Torque Control (DTC).
- **SB-PWM**: Provides users with access to the PWM outputs from the sandbox, while leveraging the dead-time generator and protection mechanisms.
- **GPO**: Offers 24x general-purpose digital outputs. These I/O pins are shared with PWM outputs.
- **GPI**: Offers 24x general-purpose inputs. These I/O pins are shared with FLT inputs.
- **FLT**: Offers 24x configurable fault inputs. These I/O pins are shared with GPI inputs.
- **DEC**: Supports the decoding of signals produced by up to four incremental position / speed encoders.
- **ETH**: Supports data exchanges on Ethernet.
- **CAN**: Provides connectivity for two separate CAN busses.
- **COM**: Implements RS422 / RS485 communication for two separate digital encoders using BiSS-C, SSI, or EnDat 2.0.
- **USR**: Provides a direct access from / to the FPGA using 36 fully-configurable high-speed I/O lanes.

### QSFP+

Four QSFP+ sockets with 4x10Gbps serial links each support **imperix RealSync** connectivity with other B-Box units for instant I/O expansion and/or precise synchronization across different controllers. Devices of previous generation, such as B-Box RCP, B-Board PRO, or TPI8032 are also compatible using forking cables (1xQSFP-to-4xSFP) at a reduced rate. Users of the FPGA sandbox can choose not to instantiate the related IP resources, so that the GTY transceivers can also be repurposed for user-defined communication applications.

### USR

36 I/O lines are available on connector B (VHDCI), which are directly fed from one of the FPGA's 3.3V bank. This offers utmost flexibility for implementing custom means of communication – including with a large parallel bus – or adding extra digital I/O capabilities to the controller.

## RJ45 ANALOG INPUTS

The B-Box 4 offers 24x analog I/O channels, available on individual RJ45 connectors. When configured as inputs, each channel supports advanced, configurable, acquisition possibilities. Notably, each channel features ultra-fast sampling, integrated over-voltage/over-current protections, multiple

filtering and down-sampling options. On the analog side, all channels guarantee over 2.7 MHz of usable bandwidth, high CMRR, and low noise performance. When used with imperix sensors, automatic configuration is possible, leveraging factory calibration information available in sensors.

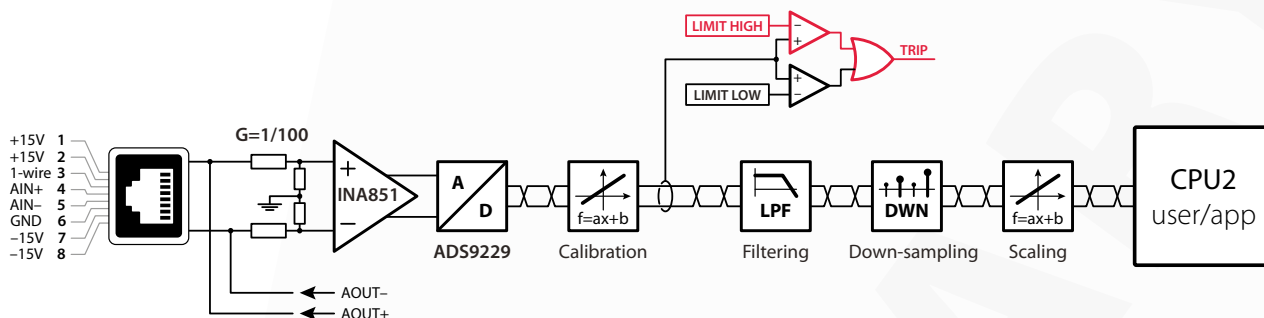


Fig. 5. Block diagram of individual analog input channels.

| Characteristic                       | Test conditions                                            | Min.   | Typ.   | Max.   | Unit   |
|--------------------------------------|------------------------------------------------------------|--------|--------|--------|--------|
| Input voltage range                  | Differential mode                                          |        | ± 10.0 |        | V      |
|                                      | Common mode input range                                    |        | ± 10.0 |        | V      |
| Maximum tolerable input voltage      | On any analog pin                                          |        | ± 25   |        | V      |
| Input impedance                      | Differential input                                         | 4.995  | 5.0    | 5.005  | kΩ     |
|                                      | Single ended input                                         |        | 3.79   |        | kΩ     |
| Signal bandwidth                     | - 3 dB, without any filter                                 |        | 2750   |        | kHz    |
| Group delay                          | Within passband                                            |        | 110    |        | ns     |
| CMRR                                 | 0 Hz – 1 MHz                                               |        | > 80   |        | dB     |
|                                      | 4 MHz                                                      |        | > 50   |        | dB     |
| Noise                                | 100 Hz – 1 MHz                                             |        | 6      |        | μV/√Hz |
| Offset                               |                                                            |        | ± 0.5  | ± 1.0  | mV     |
| Gain error                           |                                                            |        | 0.1    | 0.25   | %      |
| Sampling frequency                   | Oversampling rate (monitoring only)                        | 10     | 20     | 20     | MHz    |
|                                      | CPU rate                                                   | 1      |        | 500    | kHz    |
|                                      | FPGA rate                                                  | 1      |        | 5000   | kHz    |
| Sampling resolution                  |                                                            |        | 16     |        | bits   |
| Sampling jitter                      | Same B-Box 4                                               |        | 80     |        | ps     |
|                                      | Across several B-Boxes (≈ jitter on CLK0)                  |        | tbd    | ± 2.1  | ns     |
| Embedded power supply voltage        | $I_{OUT} < I_{OUT, max}$ (output protection not triggered) | ± 14.5 | ± 15.0 | ± 15.5 | V      |
| Embedded power supply output current | per channel                                                |        | 150    |        | mA     |
|                                      | all channels                                               |        | 2      |        | A      |

Table 2. Overall performance specifications of the analog inputs (each channel).

### INPUT-REFERRED OFFSET



Fig. 6. Statistical distribution of the offset measured on analog input.

### SENSITIVITY ERROR ON ANALOG INPUTS



Fig. 7. Statistical distribution of the sensitivity error observed on analog input.

## DIFFERENTIAL-MODE GAIN

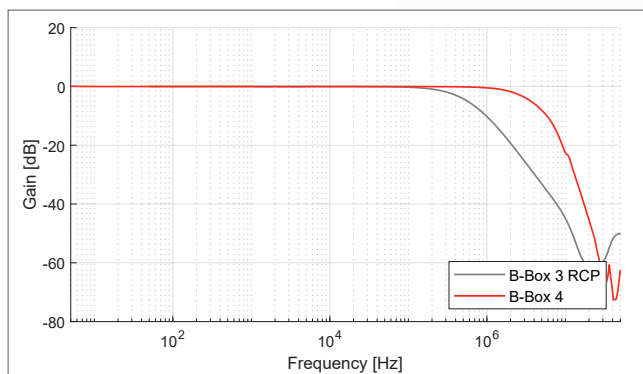


Fig. 8. Typical differential-mode gain.

## COMMON-MODE GAIN

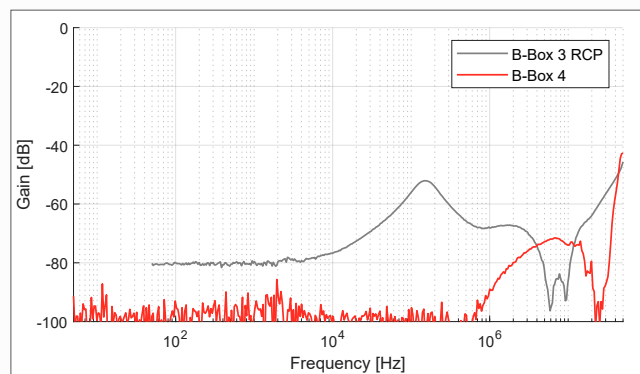


Fig. 10. Typical common mode- to differential-mode gain.

## COMMON MODE REJECTION RATIO (CMRR)

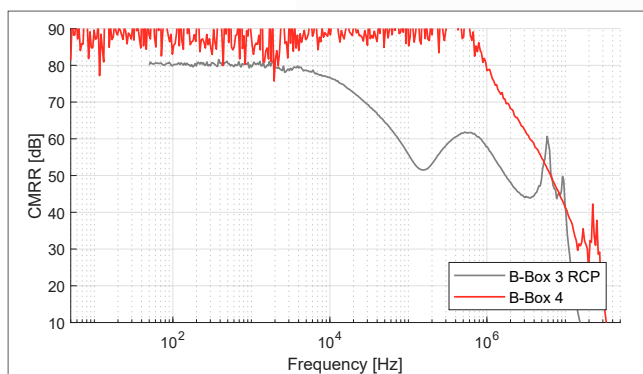


Fig. 9. Typical CMRR on analog inputs.

## INPUT-REFERRED NOISE

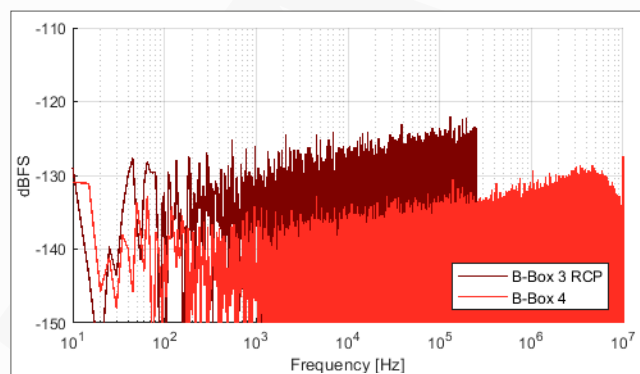


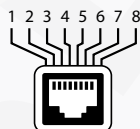
Fig. 11. Typical noise performance of analog inputs.

## ANALOG I/O CONNECTORS

Analog I/Os make use of individual RJ45 connectors. The related pinout is indicated in Table 3. Cat.6 cables with shielded twisted pairs are recommended for optimum bandwidth and EMI performance.

| Pin | Color         | Function          | Ratings                      |
|-----|---------------|-------------------|------------------------------|
| 1   | orange stripe | +15V power output | 14.5 – 15.5V<br>Max. 0.15A   |
| 2   | orange solid  |                   |                              |
| 3   | green stripe  | Reserved (1-wire) | Max. 3.5V                    |
| 4   | blue solid    | Positive input    | Max. $\pm 25V$               |
| 5   | blue stripe   | Negative input    | Max. $\pm 25V$               |
| 6   | green solid   | 0 V               | –                            |
| 7   | brown stripe  | -15V power output | -15.5 – -14.5V<br>Max. 0.15A |
| 8   | brown solid   |                   |                              |

Table 3. Pinout of imperix's RJ45 analog connectors.



Each RJ45 socket presents two colored LEDs: green to indicate the channel direction and orange to signal a potential fault. This allows for the quick identification of a trip's source. The status indicators are detailed in Table 4.

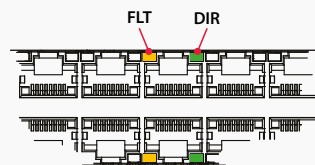


Fig. 12. Location and functions of the RJ45 LEDs.

| LED | Color  | Status             | Information                          |
|-----|--------|--------------------|--------------------------------------|
| FLT | N/A    | –                  | No fault                             |
|     | Orange | Steady             | Safety limit triggered (high or low) |
| DIR | Green  | OFF                | Channel not configured (unused)      |
|     |        | ON, steady         | Configured as input                  |
|     |        | ON, blinking (1Hz) | Configured as output                 |

Table 4. Color codes of the RJ45 LEDs.

## COMPATIBLE SENSORS

Any sensor producing a voltage output compatible with the B-Box 4's input range can be used, generally providing satisfying results. For best performance and optimum support of the oversampling, imperix nonetheless recommends using dedicated sensors with superior bandwidth and outstanding transient voltage rejection, as listed in Table 5.

| Sensor        | Type         | Range             | BW      | CMTI      | Production |
|---------------|--------------|-------------------|---------|-----------|------------|
| VSR-500-HBW   | Differential | $\pm 500 V_{pk}$  | 3 MHz   | very high | Active     |
| VSR-1000-ISO  | Isolated     | $\pm 1000 V_{pk}$ | 100 kHz | very high | Active     |
| CSR-50-HBW    | Isolated     | $\pm 50 A_{pk}$   | 1.5 MHz | very high | Active     |
| PEB-800-40 V. | Isolated     | $\pm 800 V_{pk}$  | 10 kHz  | high      | Active     |
| PEB-800-40 I. | Isolated     | $\pm 70 A_{pk}$   | 75 kHz  | high      | Active     |

Table 5. Recommended sensors for use with B-Box 4.

## SENSORS AUTO-CONFIGURATION

When using imperix sensors, as listed in Table 5, the related configuration parameters are automatically retrieved by the B-Box 4, at startup. These include factory calibration settings, when available, but at least the nominal parameters otherwise. This facilitates the hardware configuration and reduces risks of misconfiguration, while simultaneously improving measurement accuracy. The retrieved sensor parameters can be observed in the target remote view (in imperix Cockpit) or browsed directly using the front panel interface. The auto-configuration uses a dedicated 1-wire link located on pin 3 of the RJ45 connector.

## USE OF CALIBRATION DATA

When available, calibration information is automatically used to improve measurement accuracy. If for any reason, the user wishes to not to use this feature, it can be disabled:

- Directly on the B-Box 4, selecting the "analog I/O" configuration menu. Then, selecting the desired channel, and finally, "disable" in the relevant screen:



Fig. 13. Status message on the OLED screen of the B-Box 4.

- In Cockpit, unchecking the "use calibration data" checkbox in the "analog I/O" tab of the "target" configuration.

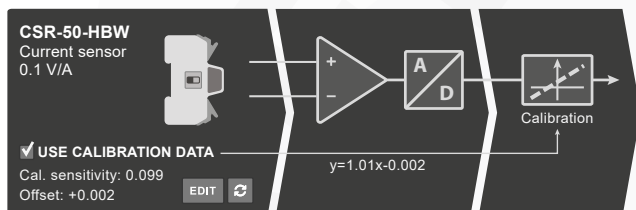


Fig. 14. Relevant section of the "analog I/O" configuration in Cockpit.

## SAFETY LIMITS

Over-voltage, over-current, or similar over-value protection is available for each channel. The corresponding protection thresholds can be configured in imperix Cockpit, or directly on the front panel. In case either of the thresholds is reached, all PWM outputs (optical and electrical) are blocked within a configurable reaction time. Fig. 16 shows the corresponding message appearing on the front panel:



Fig. 15. Information message as displayed in case of a trip.

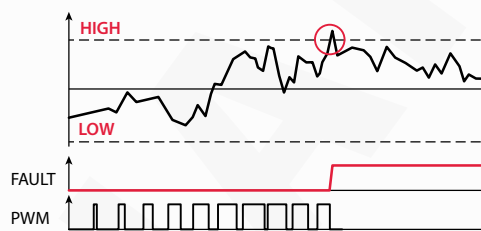


Fig. 16. Operating principle of the safety limits.

| Characteristic     | Setting    | Min.                                     | Typ.       | Max. | Unit          |
|--------------------|------------|------------------------------------------|------------|------|---------------|
| Configurable range |            |                                          | $\pm 10.0$ |      | V             |
| Setting resolution |            |                                          | 0.1        |      | V             |
| Setting accuracy   |            | $\pm 1\% \text{ m.v.} \pm 10 \text{ mV}$ |            |      |               |
| Reaction time      | ULTRA-FAST |                                          | 0.7        | 0.8  | $\mu\text{s}$ |
|                    | FAST       |                                          | 1.4        | 1.6  | $\mu\text{s}$ |

Table 6. Performance specifications of the safety limits

## FILTERING

Each channel features an optional digital low-pass filter, configurable from the front panel or from Cockpit. The possible cut-off frequencies are given in Table 7. The filter is a 5th-order Bessel filter, identical to that of the B-Box RCP<sup>3.0</sup>. Attenuation is 80 dB at 8 times the cut-off frequency.

| Cut-off frequency | Group delay        | Cut-off frequency | Group delay        |
|-------------------|--------------------|-------------------|--------------------|
| Filter OFF        | 0.0 $\mu\text{s}$  | 10 kHz            | 40 $\mu\text{s}$   |
| 0.5 kHz           | 800 $\mu\text{s}$  | 16 kHz            | 25 $\mu\text{s}$   |
| 1.0 kHz           | 400 $\mu\text{s}$  | 20 kHz            | 20 $\mu\text{s}$   |
| 1.6 kHz           | 250 $\mu\text{s}$  | 32 kHz            | 12.5 $\mu\text{s}$ |
| 2.5 kHz           | 160 $\mu\text{s}$  | 40 kHz            | 10 $\mu\text{s}$   |
| 4.0 kHz           | 100 $\mu\text{s}$  | 64 kHz            | tbd                |
| 6.4 kHz           | 62.5 $\mu\text{s}$ | 80 kHz            | tbd                |
| 8.0 kHz           | 50 $\mu\text{s}$   | 100 kHz           | tbd                |

Table 7. Possible low-pass filter (LPF) configurations.

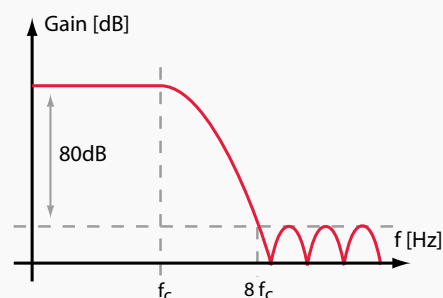


Fig. 17. Frequency response of the low-pass filter.

### OVERSAMPLED DATA PATH

The B-Box 4 always acquires as many samples as possible per control period. The number of such samples corresponds to the over-sampling ratio, which is automatically computed as the largest possible multiple of the CPU rate that is still below 20MSPs.

Oversampled data are processed in parallel to the main data path, thanks to a dedicated FPGA-based logger and stored into external RAM. When remote monitoring is active, data retrieval is handled by the supervisory linux instance.

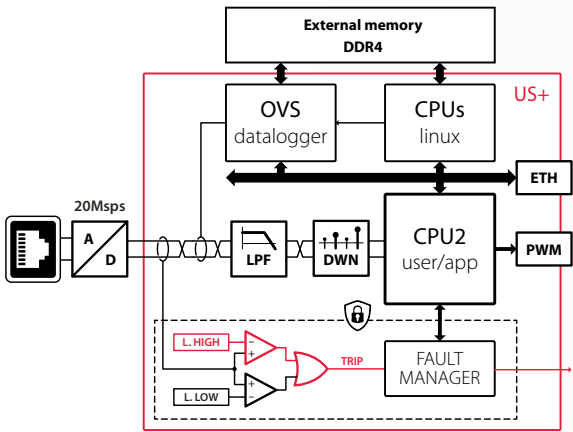


Fig. 18. Architecture of the B-Box 4's acquisition stage.

### CPU DOWN-SAMPLING CONFIGURATIONS

Multiple configurations are possible to coordinate oversampled data with slower-sampled data used within the user application. Three options are offered, which can be selected in the ADC block (with Simulink/PLECS) or C++ configuration routine:

#### 1. Synchronous sampling

This conventional method refers the sampling to SCLK, generated by phase-shifting CLK0. Typically, phase-shifts of 0° or 180° are preferred to capture current ripples precisely at the moment they attain their average value. With this approach, sampling delay is minimized. However, current non-linearities or high-frequency noise may introduce a bias in the estimation of the average current value.

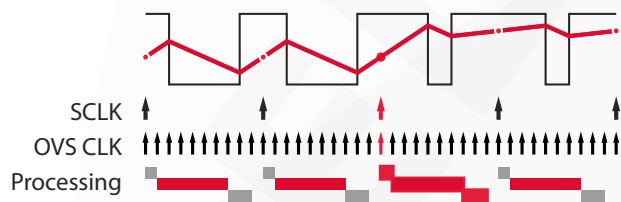


Fig. 19. Synchronous sampling, catching current ripples at the point they reach their average value.

#### 2. Synchronous averaging

This advanced technique averages numerous samples over a specific and synchronous time interval. This very effectively rejects high-frequency artifacts with minimum extra delay. Synchronous average is enabled by default on the B-Box 4.

Two averaging intervals can be configured:

- **One period of CLK0**, useful when the frequency of CLK0 is identical to that of the PWM carrier, i.e. when modulation parameters are updated once per period.
- **Two periods of CLK0**, useful when the frequency of CLK0 is twice that of the PWM carrier, i.e. when modulation parameters are updated twice per PWM period.

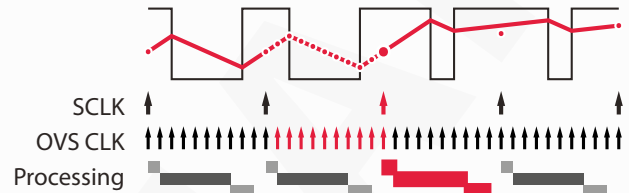


Fig. 20. Synchronous averaging configured on one period of CLK0.

Interesting, synchronous averaging improves the signal-to-noise ratio and the effective number of bits proportionally to the number of averaged samples.

| CLK0 frequency | OVS frequency | #samples | # bits | SNR |
|----------------|---------------|----------|--------|-----|
| < 312 kHz      | 20MHz         | 64       | 22     | tbc |
| < 156 kHz      |               | 128      | 23     | tbc |
| < 78 kHz       |               | 256      | 24     | tbc |
| < 39 kHz       |               | 512      | 25     | tbc |
| < 19 kHz       |               | 1024     | 26     | tbc |

Table 8. Performance specifications of the analog outputs.

When exceeding 12 analog inputs used simultaneously, the averaging process is distributed between the ADCs and the FPGA, constraining the cumulative data transfer volume. In this case, the visualization of oversampled data is restricted to 10MSPs, notwithstanding that the effective sampling rate is maintained at 20MSPs.

#### 3. Low-pass filtering + down-sampling

In the rare occasion synchronous averaging isn't sufficient to prevent the aliasing of high-frequency artifacts, implementing a digital low-pass filter on the corresponding measurement is always possible. In this case, sampling takes place on an essentially smooth waveform, at the cost of some group delay (see Table 7), which must be carefully taken into account for the selection of the right sampling instant.

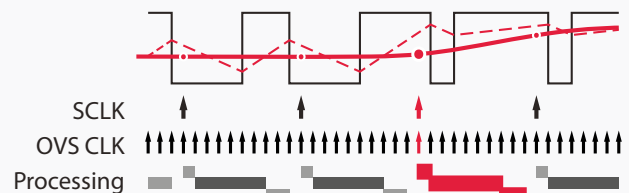


Fig. 21. Low-pass filtering with down-sampling

## RJ45 ANALOG OUTPUTS

All 24 analog I/O channels can be individually configured as analog outputs. When designated as such, an enable bit activates the operational amplifiers outputs that drive the I/O pins of the respective channel.

DAC output values are updated as fast as possible, starting from the end of the CPU control task, then latched synchronously on all channels. The latching instant may be delayed as much as one control period after the beginning of the data transfer.

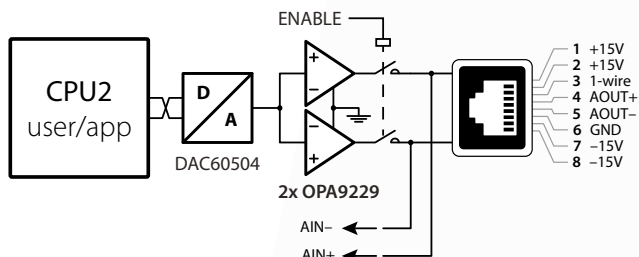


Fig. 22. Block diagram of each channel of the analog output front-end.

| Characteristic         | Setting         | Min. | Typ.       | Max.     | Unit    |
|------------------------|-----------------|------|------------|----------|---------|
| Resolution             |                 |      | 12         |          | bits    |
| Output voltage range   | Differential    |      | $\pm 10$   |          | V       |
|                        | Each pin to GND |      | $\pm 5.0$  |          | V       |
| Output current         |                 |      |            | $\pm 75$ | mA      |
| Refresh rate           |                 |      |            | 500      | ksps    |
| Settling time          |                 |      | 1.8        |          | $\mu$ s |
| Offset                 |                 |      | $\pm 0.25$ | 1.5      | mV      |
| Precision / Gain error |                 |      | $\pm 0.5$  |          | %       |

Table 9. Performance specifications of the analog outputs.

## INTERLOCK INPUT / OUTPUT

The interlock input/output connector allows coordinating emergency mechanisms across multiple B-Box units or with third-party equipment. A fault state can be either transmitted to other devices or received from external sources. The connector part number is 1786837 from Phoenix Contact. The mating part is 1790108.

In stacked B-Box configurations, interlocking is natively supported by the imperix RealSync protocol (optical fiber links).

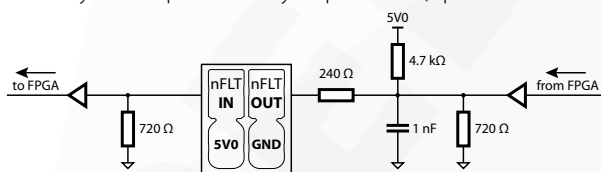


Fig. 23. Electrical circuit for the electrical inter-locking mechanism.

| Characteristic                            | Medium     | Min. | Typ. | Max. | Unit    |
|-------------------------------------------|------------|------|------|------|---------|
| Operating voltage                         | Electrical | 4.5  | 5.0  | 5.5  | V       |
| Wavelength                                | Optical    | 640  | 650  | 670  | nm      |
| Response delay to blocking of PWM signals | Optical    |      | 70   | 78   | ns      |
|                                           | Electrical |      | 40   | 50   | ns      |
|                                           | RealSync   |      | 0.25 |      | $\mu$ s |

Table 10. Performance specifications of the interlock input/output.

## DIGITAL INPUT RESOURCES

24 digital inputs are accessible via the VHDCI connectors (A) and (B). The logic voltage is selectable as either 3.3V or 5.0V, concurrently for all I/Os. Physical resources (pins) can be allocated either as GPIs or FLTs on a per channel basis. Some of them can also be used as incremental decoder inputs for the DEC peripheral. For each pin, the attribution of the corresponding software function is made based on the allocated Simulink/PLECS block, or the associated C++ routine.

| Characteristic      | Conditions   | Min. | Typ. | Max. | Unit |
|---------------------|--------------|------|------|------|------|
| Operating voltage   | 5.0V         | 4.5  | 5.0  | 5.5  | V    |
|                     | 3.3V         | 3.0  | 3.3  | 3.6  | V    |
| Operating data rate | 5.0V         |      |      | 400  | Mbps |
|                     | 3.3V         |      |      | 350  | Mbps |
| Propagation delay   | 3.3V or 5.0V | 0.7  | <1.5 | 23.4 | ns   |

Table 11. Performance specifications of the digital inputs.

## GENERAL-PURPOSE INPUTS (GPI)

When the physical resource (pin) is used by a GPI function, any bit can be readily accessed via the associated Simulink / PLECS block or the C++ routine.

## FAULT FEEDBACK INPUTS (FLT)

When the physical resource (pin) is used by a FLT function, its value can be easily accessed via the associated Simulink / PLECS block or the C++ routine. Besides, any raising transition from logic '0' to '1' instantly triggers a FAULT, similarly to other sources.

| Characteristic                            | Min. | Typ. | Max. | Unit |
|-------------------------------------------|------|------|------|------|
| Response delay to blocking of PWM signals |      | 50   | 60   | ns   |

Table 12. Performance specifications of the fault feedback inputs.

## INCREMENTAL DECODER INPUTS (DEC)

Digital inputs of the B-Box 4 further supports quadrature signal inputs for speed/position sensor signals (usually called A and B), with or without a reset line (usually called Z). These inputs are either configurable as four independent inputs or two differential inputs.

Each DEC module counts all 4 edges of the A and B inputs, leading to an angular resolution 4 times superior to the PPR value. The position counter can be reset either at a specified value, or using the Z signal provided by the sensor.

When using DEC inputs, the position is latched at the same time as ADC inputs are sampled.

| Pin | GPI signal | DEC signal            | Pin | GPI signal | DEC signal            |
|-----|------------|-----------------------|-----|------------|-----------------------|
| A2  | GPI0       | A0                    | B2  | GPI8       | A2                    |
| A3  | GPI1       | B0                    | B3  | GPI9       | B2                    |
| A4  | GPI2       | Z0                    | B4  | GPI10      | Z2                    |
| A5  | GPI3       | A1 or $\overline{A0}$ | B5  | GPI11      | A3 or $\overline{A2}$ |
| A6  | GPI4       | B1 or $\overline{B0}$ | B6  | GPI12      | B3 or $\overline{B2}$ |
| A7  | GPI5       | Z1 or $\overline{Z0}$ | B7  | GPI13      | Z3 or $\overline{Z2}$ |
| A8  | GPI6       | N/A                   | B8  | GPI14      | N/A                   |
| A9  | GPI7       | N/A                   | B9  | GPI15      | N/A                   |

Table 13. Signal assignment for the GPI/DEC inputs.

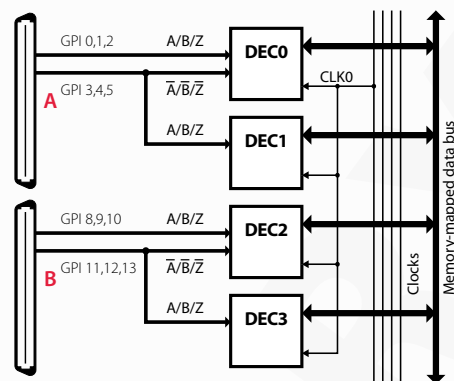


Fig. 24. Device mapping and configuration of the four incremental speed/position sensors decoders.

| Characteristic   | Test conditions                                                                                                                                                            | Min. | Typ. | Max. | Unit |
|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| Input signals    | <ul style="list-style-type: none"> <li>Single-ended signaling: A, B and Z (Z is optional)</li> <li>Differential signaling: A, A, B, B, Z, Z (Z, Z are optional)</li> </ul> |      |      |      |      |
| Sampling options | Either synchronized with ADC, or independent                                                                                                                               |      |      |      |      |
| PPR frequency    | Quadruple rate.                                                                                                                                                            | 0    |      | 5    | MHz  |

Table 14. Performance specifications of the DEC block.

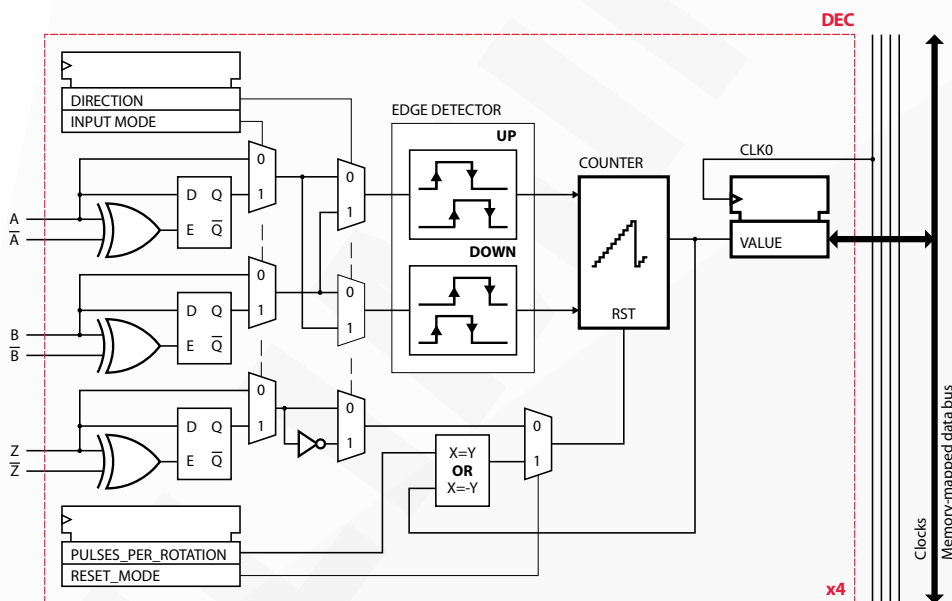


Fig. 25. Device mapping and configuration of the four incremental speed/position sensors decoders.

## ELECTRICAL INPUTS / OUTPUTS

Electrical digital inputs are grouped on the (A) and (B) high-speed connectors (part number: TE 5787962-1).

The following functions are available:

- **GPI/FLT** (24 bits): General purpose or fault feedback inputs.
- **USR** (32+4 bits): Fully-configurable input/output bus.

Equivalently, electrical digital outputs are grouped on the (C) and (D) connectors (part number: TE 5787962-1).

The following functions are available:

- **GPO/PWM** (48 bits): General purpose outputs or pulse-width modulated outputs (PWM).

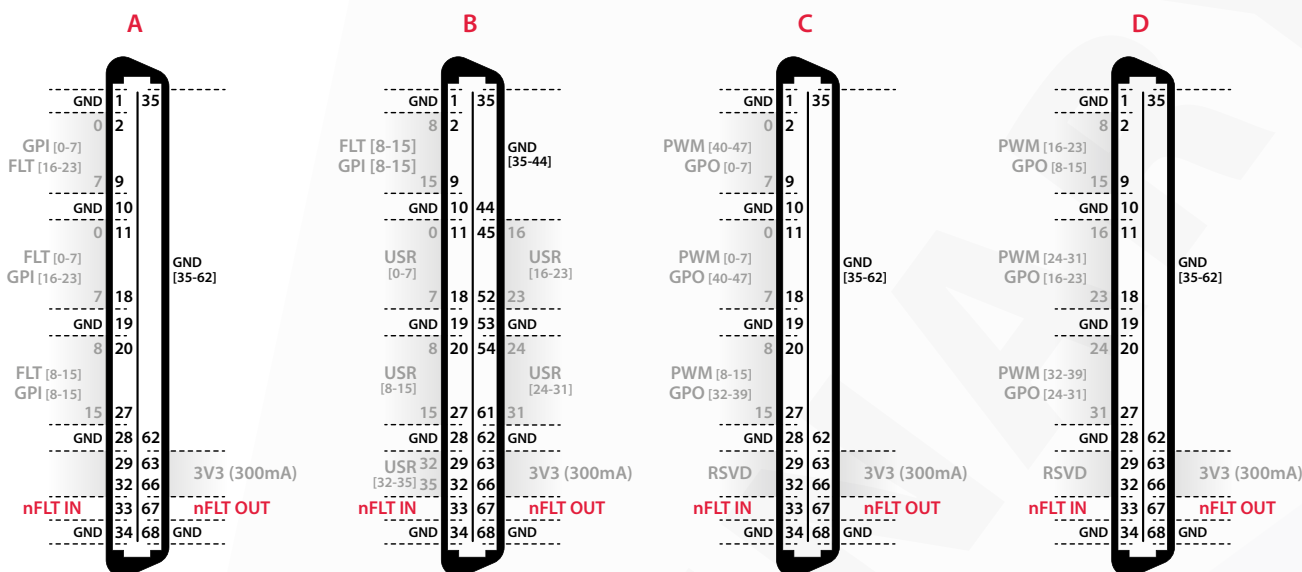


Fig. 45. Pinout of the rear-side VHDCI HD68 connectors.

The VHDCI connector pinout differs slightly from that of the B-Box RCP <sup>3.0</sup> as it features some overlap on GPI/FLT and GPO/PWM pins to support a larger bus widths. Nonetheless, pin-to-pin compatibility remains guaranteed.

| Pin               | FPGA  | Functions   |
|-------------------|-------|-------------|
| <b>INPUTS (A)</b> |       |             |
| 2                 | DI 0  | GPI0/FLT16  |
| ...               | ...   | ...         |
| 9                 | DI 7  | GPI7/FLT23  |
| 11                | DI 16 | GPI16/FLT0  |
| ...               | ...   | ...         |
| 18                | DI 23 | GPI23/FLT7  |
| 20                | DI 8  | GPI8/FLT8   |
| ...               | ...   | ...         |
| 27                | DI 15 | GPI15/FLT15 |
| 33                |       | nFLT_in     |
| 67                |       | nFLT_out    |

Table 36. Pinout of the VHDCI connectors (A) and (B).

| Pin               | FPGA            | Functions       |
|-------------------|-----------------|-----------------|
| <b>INPUTS (B)</b> |                 |                 |
| 2                 | DI 8            | FLT 8 / GPI 8   |
| ...               | ...             | ...             |
| 9                 | DI 15           | FLT 15 / GPI 15 |
| 11-18             | USR 0 - USR 7   |                 |
| 20-27             | USR 8 - USR 15  |                 |
| 29-32             | USR 32 - USR 35 |                 |
| 45-52             | USR 16 - USR 23 |                 |
| 51-61             | USR 24 - USR 31 |                 |
| 33                |                 | nFLT_in         |
| 67                |                 | nFLT_out        |

| Pins               | FPGA  | Functions       |
|--------------------|-------|-----------------|
| <b>OUTPUTS (C)</b> |       |                 |
| 2                  | DO 40 | PWM 40 / GPO 0  |
| ...                | ...   | ...             |
| 9                  | DO 47 | PWM 47 / GPO 7  |
| 11                 | DO 0  | PWM 0 / GPO 40  |
| ...                | ...   | ...             |
| 18                 | DO 7  | PWM 7 / GPO 47  |
| 20                 | DO 8  | PWM 8 / GPO 32  |
| ...                | ...   | ...             |
| 27                 | DO 15 | PWM 15 / GPO 39 |
| 33                 |       | nFLT_in         |
| 67                 |       | nFLT_out        |

Table 37. Pinout of the VHDCI connectors (C) and (D).

| Pins               | FPGA  | Functions       |
|--------------------|-------|-----------------|
| <b>OUTPUTS (D)</b> |       |                 |
| 2                  | DO 16 | PWM 16 / GPO 8  |
| ...                | ...   | ...             |
| 9                  | DO 23 | PWM 23 / GPO 15 |
| 11                 | DO 24 | PWM 24 / GPO 16 |
| ...                | ...   | ...             |
| 18                 | DO 31 | PWM 31 / GPO 23 |
| 20                 | DO 32 | PWM 32 / GPO 24 |
| ...                | ...   | ...             |
| 27                 | DO 39 | PWM 39 / GPO 31 |
| 33                 |       | nFLT_in         |
| 67                 |       | nFLT_out        |

| Main function | Alternate function | Location | Max. speed | Internal topology                                | Voltage                            |
|---------------|--------------------|----------|------------|--------------------------------------------------|------------------------------------|
| GPI           | 0-7                | FLT      | > 200Mbps  | Level-shifted down to 1V8                        | Selectable voltage<br>3.3V or 5.0V |
|               | 8-15               |          |            |                                                  |                                    |
|               | 16-23              |          |            |                                                  |                                    |
| PWM           | 0-7                | GPO      | > 200Mbps  | Level-shifted from 3V3<br>Level-shifted from 1V8 |                                    |
|               | 8-15               |          |            |                                                  |                                    |
|               | 16-23              |          |            |                                                  |                                    |
|               | 24-31              |          |            |                                                  |                                    |
|               | 32-39              |          |            |                                                  |                                    |
|               | 40-47              |          |            |                                                  |                                    |
| USR           | 0-35               | N/A      | > 400Mbps  | Straight from/to FPGA                            | <b>WARNING</b> Always 3.3V !       |

Table 38. Availability of FPGA resources on the VHDCI and optical output connectors.

### WARNING:

Always make sure to apply and use the **appropriate voltage level** on each signal. Unexpected behavior or damage may occur in case of inappropriate voltage. The operating logic voltage can be easily selected using the selector switch on the rear side of the B-Box 4 unit. **This applies to both GPI /FLT and GPO /PWM.**

3.3V logic



5.0V logic



## BIDIRECTIONAL DIGITAL I/O RESOURCES

### USER-CONFIGURABLE I/O BUS (USR)

The B-Box 4 offers high-speed connectivity for custom FPGA implementations, thanks to 36 bidirectional I/O lines offered on connector (B), which are directly tied to the System-on-Chip (Ultrascale+ 7EV).

| Characteristic                  | Min. | Typ. | Max. | Unit     |
|---------------------------------|------|------|------|----------|
| Operating data rate (all lanes) |      |      | 400  | Mbps     |
| Current-limiting resistors      |      | 33   |      | $\Omega$ |
| Operating voltage               | 3.0  | 3.3  | 3.6  | V        |

Table 15. Performance specifications of the USR bus.

### DIGITAL OUTPUT RESOURCES

Similar to digital inputs, 48 digital outputs are accessible via the VHDCI connectors (C) and (D). The logic voltage is selectable as either 3.3V or 5.0V, concurrently for all I/Os. Physical resources (pins) can be allocated either as PWMs or GPOs on a per channel basis. The 24 first lanes are also produced on optical emitters for superior EMI performance. For each pin, the attribution of the corresponding function is determined by the instantiated Simulink/PLECS block, or the associated C++ routine.

#### WARNING:

On the B-Box 4, given the potential use of any GPO/PWM pin as a gate driving signal, all digital outputs are always tied to a logic '0' when the B-Box is not operating normally (i.e. including during boot, FPGA flashing, or similar situations). However, FAULT conditions (e.g. overvalues) and the 'enable/disable' PWMs function (in Cockpit) only affects outputs allocated as PWM lanes.

| Characteristic                                                            | Test conditions          | Min. | Typ.      | Max.      | Unit |
|---------------------------------------------------------------------------|--------------------------|------|-----------|-----------|------|
| Rise/fall time                                                            | 3.3V, 1M $\Omega$   15pF |      | 1.9       |           | ns   |
| Max. output current                                                       | 3.3V                     |      |           | $\pm 50$  | mA   |
| Propagation delay                                                         |                          | 0.8  | <1.0      | 7.4       | ns   |
| Propagation delay asymmetry ( $t_{PLH} - t_{PHL}$ and channel-to-channel) | Same unit                | –    | $\pm 0.2$ | $\pm 3.3$ | ns   |
|                                                                           | Two units, B-Box 4       |      | $\pm 1.5$ | $\pm 5.3$ | ns   |
|                                                                           | Mix of B-Box 4 and BB3   |      | $\pm 1.7$ | $\pm 5.8$ | ns   |
| Relative jitter                                                           | Same unit                |      | tbc       |           | ps   |
|                                                                           | Two units, B-Box 4       |      | tbc       |           | ps   |
| Phase noise                                                               |                          |      | tbc       |           | ns   |

Table 16. Performance specifications of the electrical outputs at 3.3V.

| Characteristic                                                            | Test conditions          | Min. | Typ.      | Max.      | Unit |
|---------------------------------------------------------------------------|--------------------------|------|-----------|-----------|------|
| Rise/fall time                                                            | 5.0V, 1M $\Omega$   15pF |      | 1.8       |           | ns   |
| Max. output current                                                       | 5.0V                     |      |           | $\pm 50$  | mA   |
| Propagation delay                                                         |                          | 0.5  | <1.0      | 7.1       | ns   |
| Propagation delay asymmetry ( $t_{PLH} - t_{PHL}$ and channel-to-channel) | Same unit                | –    | $\pm 0.2$ | $\pm 3.3$ | ns   |
|                                                                           | Two units, B-Box 4       |      | $\pm 1.5$ | $\pm 5.3$ | ns   |
|                                                                           | Mix of B-Box 4 and BB3   |      | $\pm 1.7$ | $\pm 5.8$ | ns   |
| Relative jitter                                                           | Same unit                |      | tbc       |           | ps   |
|                                                                           | Two units, B-Box 4       |      | tbc       |           | ps   |
| Phase noise                                                               |                          |      | tbc       |           | ns   |

Table 17. Performance specifications of the electrical outputs at 5.0V.

### GENERAL-PURPOSE OUTPUTS (GPO)

When the physical resource (pin) is used by a GPO function, any bit can be directly imposed by the associated Simulink/PLECS block or the C++ routine.

### ELECTRICAL PWM OUTPUTS (PWM)

When configured as PWM outputs, odd and even lanes are associated by default as a pair, constituting a so-called PWM channel. One or several channels may then be allocated by a given modulator, depending on its type, depending on the instantiated Simulink/PLECS block, or the configuration set by the associated C++ routine.

For each channel, three PWM coding styles are possible:

- **PWMH + PWML**: high- and low-side gate drive signals, i.e. pseudo-complementary signals with a configurable dead time between their '1' states.
- **PWM + ACTIVE**: PWM and 'activation' signals, i.e. one signal coding the switching state and one coding the blocking/unblocking of the operation.
- **INDEPENDENT**: the two PWM lanes are driven by two independent PWM modulators. In this case, no PWM channel is formed and no dead time is enforced.

With pseudo-complementary operation (PWMH + PWML), a dead time can be configured in the relevant Simulink/PLECS blocks or using the corresponding C++ routine.

### OPTICAL PWM OUTPUTS (PWM)

While all PWM/GPO digital outputs are available as electrical signals on the VHDCI connectors (C) and (D), a subset of those lanes is simultaneously driving 650nm plastic optical fiber outputs (part number FT50MHNR) on the front side of the B-Box 4. The available signals are PWM0-PWM23, which also correspond to GPO8-15 and GPO32-47 (see Table 38).

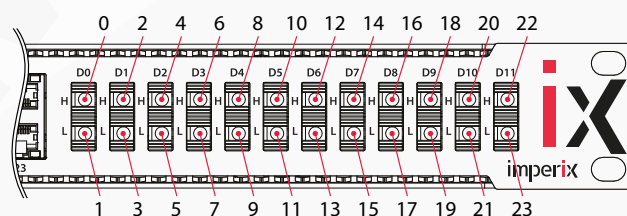


Fig. 26. Physical assignment of PWM lanes.

The overall timing accuracy of the optical outputs is shown in Table 18, including all sources of uncertainty up to the fibers, i.e. including device-to-device synchronization. Additional details clock generation are given on (page 12).

| Characteristic              | Test conditions                               | Min. | Typ. | Max.     | Unit |
|-----------------------------|-----------------------------------------------|------|------|----------|------|
| Wavelength                  |                                               | 640  | 650  | 670      | nm   |
| Propagation delay           | FPGA to FR50MHNR receiver with 1m fiber       |      | tbc  | tbc      | ns   |
| Phase noise                 | FPGA to FR50MHNR receiver with 1m fiber       |      | tbc  | tbc      | ps   |
| Propagation delay asymmetry | Any two signals, same B-Box 4                 |      | tbc  | tbc      | ns   |
|                             | Any two signals, across all networked B-Boxes |      | tbc  | $\pm 15$ | ns   |

Table 18. Performance specification of the optical PWM outputs.

## CAN-FD TRANSCEIVERS (CAN A/B)

Two Controller Area Network (CAN) transceivers are embedded inside the B-Box 4, supporting CAN 2.0A/B. Connectivity is provided using RJ45 connectors on the rear side of the device. The devices support the flexible data rate option (suffix -FD) for extended support, including:

- Possibility to add a second bitrate: the data bitrate
- Addition of a BRS (Bit Rate Switch) flag to optionally enable the second bitrate
- Support for payloads up to 64 bytes

| Protocol variant  | Identifier | Payload    | Max. bitrate | Max. data bitrate |
|-------------------|------------|------------|--------------|-------------------|
| Standard CAN 2.0A | 11-bit     | ≤ 8 Bytes  | 1 Mbps       | N/A               |
| Extended CAN 2.0B | 29-bit     | ≤ 8 Bytes  | 1 Mbps       | N/A               |
| Standard CAN-FD   | 11-bit     | ≤ 64 Bytes | 1 Mbps       | 5 Mbps            |
| Extended CAN-FD   | 29-bit     | ≤ 64 Bytes | 1 Mbps       | 5 Mbps            |

Table 19. Supported protocol variants on the two CAN-FD modules.

| Characteristic                          | Min. | Typ. | Max. | Unit |
|-----------------------------------------|------|------|------|------|
| Arbitration bit rate                    |      |      | 1.0  | Mbps |
| Data bit rate (CAN-FD)                  |      |      | 5.0  | Mbps |
| Tolerable voltage on CAN+ and CAN- pins | -27  |      | +40  | V    |
| Bus impedance                           | 119  | 120  | 123  | Ω    |

Table 20. Performance specifications for the CAN-FD transceivers.

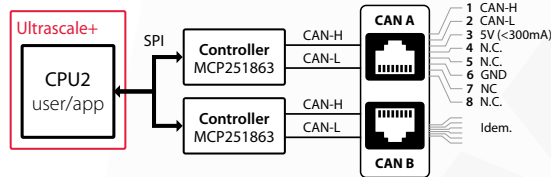


Fig. 27. Block diagram of the CAN-FD interfaces.

| Pin | Color         | Description     | Pin | Color        | Description |
|-----|---------------|-----------------|-----|--------------|-------------|
| 1   | orange stripe | CAN H           | 5   | blue stripe  | N.C.        |
| 2   | orange solid  | CAN L           | 6   | green solid  | GND         |
| 3   | green stripe  | 5V (max. 300mA) | 7   | brown stripe | N.C.        |
| 4   | blue solid    | N.C.            | 8   | brown solid  | N.C.        |

Table 21. Pin assignments on the CAN A/B RJ45 connectors.

### WARNING:

The B-Box 4 does not include built-in terminations on its CAN bus lines. External 120Ω resistors may be required.

## DIGITAL ENCODER INPUTS (SERIAL A/B)

The B-Box4 offers two RS-485-based hardware modules that support communication with position encoders and other similar digital sensors. The integrated FPGA drivers are configurable for SSI, BiSS-C, and EnDat 2.2 communication protocols, on a per-channel basis. All three drivers support data streams with up to 32-bit single and multi-turn resolution at the highest transmission clock frequency specified by the standards.

| Protocol  | Single-turn resolution | Multi-turn resolution | Max. transmission clock rate |
|-----------|------------------------|-----------------------|------------------------------|
| SSI       | ≤ 32 bits              | ≤ 32 bits             | 2 MHz (*)                    |
| BiSS-C    | ≤ 32 bits              | ≤ 32 bits             | 10 MHz (*)                   |
| EnDat 2.2 | ≤ 32 bits              | ≤ 32 bits             | 16 MHz (*)                   |

Table 22. SSI, BiSS-C and EnDat2.2 payload and clock frequency specifications. (\*) as defined by the standards

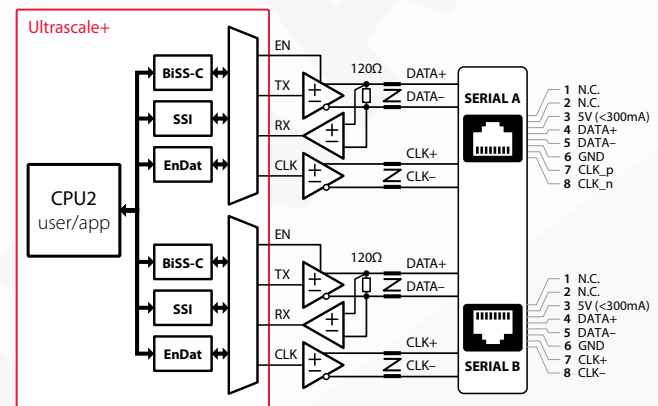


Table 23. Block diagram of the digital encoder interfaces.

| Pin | Color         | Description | Pin | Color        | Description |
|-----|---------------|-------------|-----|--------------|-------------|
| 1   | orange stripe | N.C.        | 5   | blue stripe  | DATA-       |
| 2   | orange solid  | N.C.        | 6   | green solid  | GND         |
| 3   | green stripe  | GND         | 7   | brown stripe | CLK+        |
| 4   | blue solid    | DATA+       | 8   | brown solid  | CLK-        |

Table 24. Pin assignments on the SERIAL A/B RJ45 connectors.

| Module | Signal | Sandbox         | FPGA pin |
|--------|--------|-----------------|----------|
| A      | CLK    | private_out(49) | C19      |
|        | EN     | private_out(50) | B20      |
|        | TX     | private_out(51) | A22      |
|        | RX     | private_in(96)  | A19      |
| B      | CLK    | private_out(52) | AM21     |
|        | EN     | private_out(53) | AL21     |
|        | TX     | private_out(54) | AF22     |
|        | RX     | private_in(97)  | AG23     |

Table 25. FPGA resource assignment of the SERIAL A/B interfaces.

## CLOCKS AND INTERRUPTS GENERATOR

The B-Box 4 employs a timing architecture distinct from that of most microcontrollers and rapid prototyping systems. To ensure maximum flexibility and precise clock dissemination and synchronization across multiple controllers, all timing resources are ultimately derived from a unique 250 MHz time base within the top master controller. This enables bringing all resources inside the same clock domain, thereby avoiding any potential clock drift.

From that time base, four independent clock generators are available, which can be allocated to FPGA resources – such as ADC and PWM – and subsequently trigger CPU events. In networked configurations, these four clocks are automatically disseminated, synchronized and aligned, thereby constituting common references.

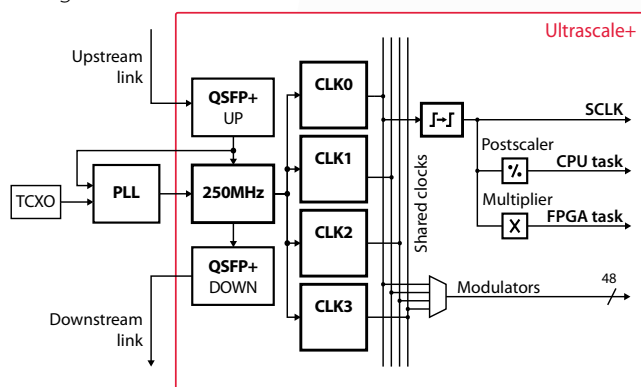


Fig. 28. Clock generation system inside the B-Box 4.

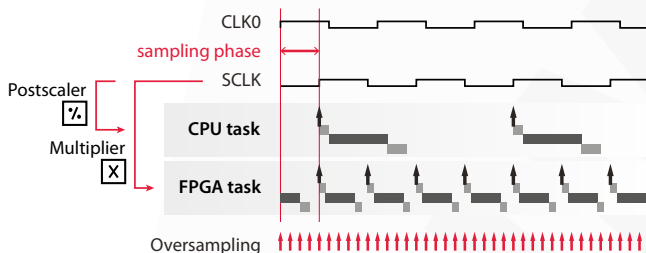


Fig. 29. Derivation of the interrupts for the CPU and FPGA control tasks.

CLK0 holds a special status as it is always active. It serves as the clock source for generating essential events, including:

- The sampling strobe SCLK with a configurable phase-shift.
- The launch of the CPU task, based on SCLK, once all data are ready for processing. A "postscaler" coefficient (integer) is also available to decimate (reduce the rate of) the processing actions relative to the sampling rate.
- The launch of the FPGA task, also based on SCLK. A "multiplier" parameter is available for increased flexibility.

CLK1 to CLK3 are optional, configurable clock sources. They support glitch-free re-configuration during runtime as to allow variable-frequency operation.

| Characteristic                     | Object    | Value          |
|------------------------------------|-----------|----------------|
| Counter resolution                 |           | 4.0ns          |
| Counter depth (carrier, prescaler) |           | 16 bits        |
| Postscaler value                   |           | 0 – 65'535     |
| Multiplier value                   |           | 0 – 100'000    |
| Achievable frequency range         | CLK0-CLK3 | 58.2mHz-125MHz |
|                                    | CPU task  | 50Hz-500kHz    |
|                                    | FPGA task | 50Hz-5MHz      |

Table 26. Performance specifications of the clock generation system.

In multi-unit configurations – including with B-Boxes of previous generation – all clocks are automatically natively synchronized and synchronized. This guarantees the consistency of all timings throughout the control network, notably:

- Synchronicity of the ADC sampling events
- Accuracy of phase-shifts between any ADC or PWM events

Typical performance is shown in Table 27 and Fig. 30.

| Characteristic                             | Min. | Typ. | Max. | Unit |
|--------------------------------------------|------|------|------|------|
| Mean deviation, any slave B-Box vs. master | -2.0 | 0    | 2.0  | ns   |
| Phase noise (jitter), any B-Box            |      |      | ±230 | ps   |

Table 27. Synchronization performance of CLK peripheral blocks across multiple B-Boxes using imperix RealSync.

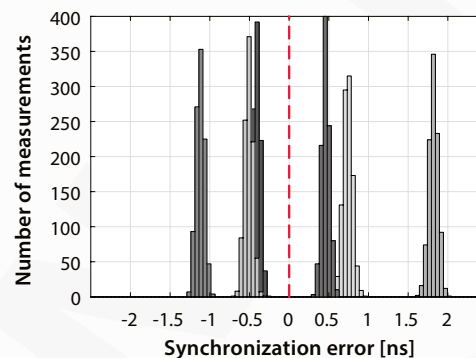


Fig. 30. Relative phase error performance with several B-Boxes in a stacked configuration (example with 6 slaves units).

## PULSE WIDTH MODULATORS

The B-Box 4 features a powerful Pulse-Width Modulation system that includes five different modulator types, which can be freely assigned across up to 48 PWM outputs. Figure 30 illustrates this structure.

- **48x CB-PWM**: Carrier-based modulators for 24 channels or up to 48 individual lanes. These modulators support various carrier types and both single and double update rate. CB-PWM blocks also provides the necessary FPGA support for space-vector modulator blocks (SV-PWM).
- **2x PP-PWM**: Programmed patterns modulators (2x three-phase). These modulators support the implementation of Selective Harmonic Elimination (SHE) or other types of Optimized Pulse Patterns (OPP), including for multilevel modulation patterns.
- **1x DO-PWM**: Direct output (48bits) from the user application (CPU) with minimum latency. Unlike GPOs, DO-PWM outputs can use the dead time generator and benefit from the safety mechanisms and PWM 'enable / disable' actions in Cockpit. This notably supports software-based modulation techniques such as finite control set MPC.
- **3x SS-PWM**: Sort-&-Select modulation and balancing for up to 3 arms of up to 12 modules each. This sub-system offers hardware-level support for the operation of Modular Multilevel Converters or similar topologies.
- **1x SB-PWM**: This subsystems connects with the user-programmable area inside the FPGA (sandbox). This is typically useful for developing full-custom modulation techniques, while still leveraging imperix's protection mechanisms and PWM 'enable / disable' actions in Cockpit.

At the output of the modulators, each of the 48 PWM signals can be directly propagated to the physical outputs (electrical or optical), or to go through a dead time generator (see Fig. 31). Finally, the high-resolution blocks implement fine tuning of the signal edges, when used in conjunction with CB-PWM

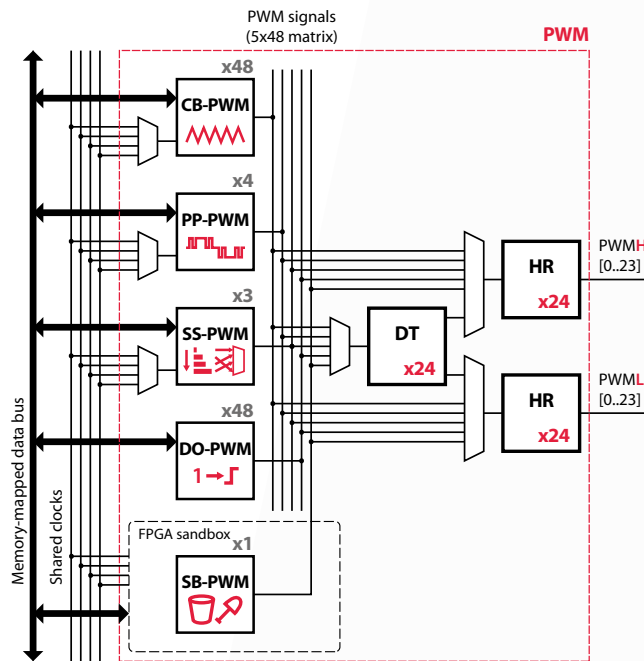


Fig. 31. Internal structure of the PWM signals generation system.

## DEAD TIME GENERATOR

As depicted by Fig. 31, PWM resources are supplemented by a dedicated dead time generator at their outputs. This subsystem can be optionally bypassed for single-lane operation. The dead time generation process relies on a finite state machine (illustrated in Fig. 42). Operationally, it delays the rising edge of both the high-side and low-side signals by a configurable duration. This results in an effective propagation delay equivalent to half the dead time. By design, this implementation intrinsically prevents the generation of '1:1' states, as well as any pulse shorter than the set dead time value.

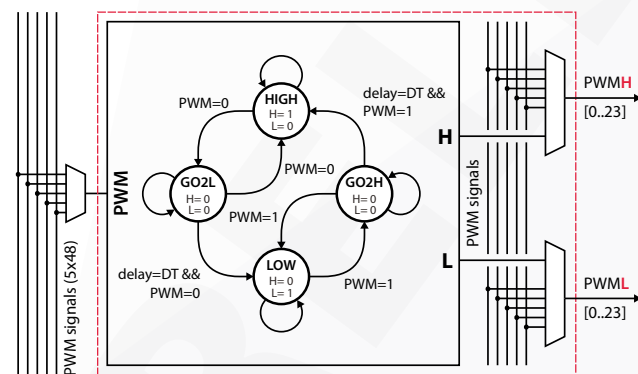


Fig. 32. Internal structure of the dead time generation block.

| Characteristic       | Min.  | Typ. | Max. | Unit |
|----------------------|-------|------|------|------|
| Dead time resolution |       | 4    |      | ns   |
| Dead time value      | 0.004 |      | 262  | μs   |

Table 28. Performance specifications of the dead time generation.

## HIGH-RESOLUTION EDGE-SHIFT OUTPUTS

In the B-Box 4, modulators are supplemented by high-resolution (HR) edge-shift blocks, which enable fine edge adjustments in steps as small as 250ps. This resolution is achieved by utilizing phase-shifted derivatives of the 250 MHz clock, which effectively increases the time resolution on the generation of signal edges by a factor of 16. High-resolution mode is only available in conjunction with CB-PWM. It can be applied to either the phase or the duty-cycle, but not both simultaneously.

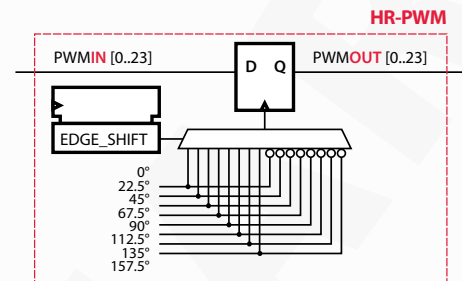


Fig. 33. Internal structure of CB-PWM peripheral blocks.

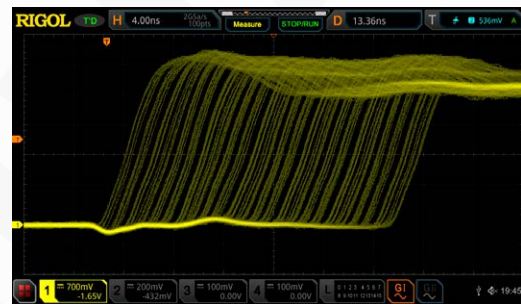


Fig. 34. PWM edges with high-resolution output mode.



Fig. 35. PWM edges with standard-resolution output mode.

## CB-PWM: CARRIER-BASED MODULATION

Carrier-based modulators provide the simplest method for generating pulse-width modulated signals. The corresponding block features 48 independent modulators, each offering independent control over duty-cycle and phase parameters, along with a choice of four different carrier types. Although the duty-cycle and phase can be written by the CPU at any moment, these parameters are only latched at the bottom of the carrier cycle. When using triangular carriers, the modulators can be configured for either single or double update rates (update at both the top and bottom of the carrier). When high-resolution mode is enabled, PWM signal edges are adjusted thanks to the HR-PWM block, based on:

- The duty-cycle when the phase is defined as a constant.
- The phase otherwise, including when both parameters are real-time tunable variables.

| Characteristic                            | Standard resolution | High resolution |
|-------------------------------------------|---------------------|-----------------|
| Counter depth                             | 16 bits             | 20 bits         |
| Phase-shift resolution (all carriers)     | 4 ns                | 250 ps          |
| Duty-cycle resolution (sawtooth carriers) | 4 ns                | 500 ps          |
| Duty-cycle resolution (triangle carriers) | 8 ns                | 500 ps          |

Table 29. Performance specifications of the CB-PWM blocks.

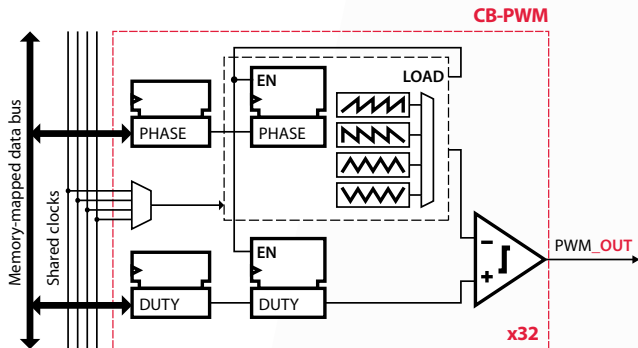


Fig. 36. Internal structure of CB-PWM peripheral blocks.

### SV-PWM: SPACE VECTOR MODULATION

Space vector modulation (SV-PWM, sometimes also referred to as SVM) is fully supported via dedicated software drivers, leveraging the same FPGA resources as the CB-PWM subsystem. Two- and three-level converter topologies are supported, with single or double update per PWM period. SV-PWM blocks automatically allocate adjacent lanes or channels.

### DO-PWM: DIRECT OUTPUT ACCESS

The DO-PWM subsystem provides direct access to the PWM outputs from the user application. Unlike other output peripherals, the CPU immediately works to toggle the desired output rather than transferring a full buffer to the FPGA. This design sacrifices time-coherency (across several outputs) in favor of minimum latency, which is beneficial for time-sensitive techniques like Model Predictive Control (MPC) or hysteresis control.

Similarly to all PWMs and unlike GPO signals, DO-PWM outputs get inhibited by safety mechanisms in case of trip. They can also benefit from the dead-time generator block when configured as a channel.

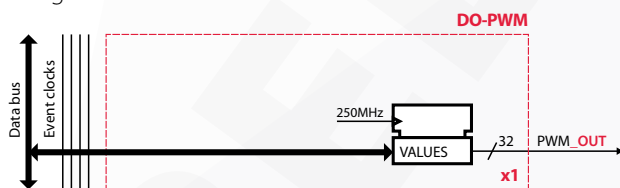


Fig. 37. Internal structure of the DO-PWM block.

### PP-PWM: PROGRAMMED PATTERNS MODULATION

The Programmed Pattern (PP-PWM) modulation blocks are dedicated to techniques that rely on pre-computed switching instants. This includes the generation of firing angles for thyristor-based converters, or the implementation of PWM with Selective Harmonic Elimination (SHE) or using any other set of Optimized Pulse Patterns (OPP). PP-PWM blocks accelerate the run-time execution of optimized patterns but do not support their selection or optimization (whether online or offline).

PP-PWM blocks are designed to operate with a fixed counter period and therefore a fixed angular resolution. However, they can be fed by a variable-frequency clock (see the CLK peripheral block), enabling their implementation within software PLLs. Each PP-PWM block incorporates several Look-Up Tables (LUTs) for switching angles, along with dedicated registers for switching event direction (up or down) and an additional truth table for decoding the output state.

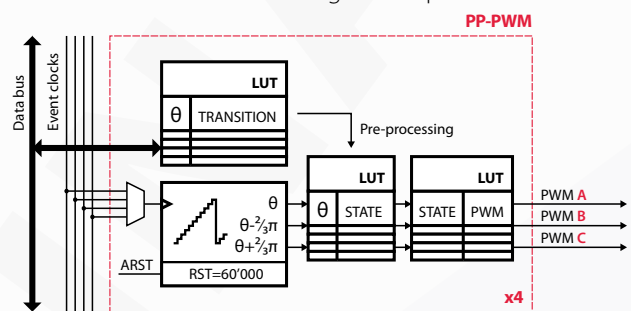


Fig. 38. Internal structure of the SS-PWM block.

| Characteristic                                             | Value                  |
|------------------------------------------------------------|------------------------|
| Number of angle registers (values 0 – 60'000)              | 3x 16 angles x 16 bits |
| Number of transition direction bits registers (up or down) | 3x 16 bits             |
| Size of output LUT                                         | 64 angles (for 90°)    |
| Edge resolution (respectively to signal period)            | 0.017 ‰                |

Table 30. Performance specifications of the PP-PWM block.

### SB-PWM: PWM ACCESS FROM THE SANDBOX

In addition to pre-implemented modulators, the B-Box 4 also supports the implementation of full-custom modulation techniques via the FPGA sandbox. On the CPU side, SBI and SBO blocks offer read/write access from/to the CPU. On the hardware side, PWM lanes can be connected to the physical outputs through the dead-time generator block (see Fig. 31) as well as safety-related functions.

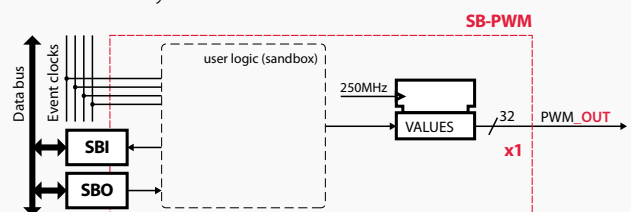


Fig. 39. Internal structure of SB-PWM blocks.

## SS-PWM: SORT-AND-SELECT MODULATION FOR MODULAR MULTILEVEL CONVERTERS (MMC)

SS-PWM blocks provide firmware-level support for modulation with integrated voltage balancing, specifically designed for multilevel converters. This applies to Modular Multilevel Converters (MMCs), but also to similar topologies that utilize floating submodules. The SS-PWM subsystem accesses the submodule voltages acquired via analog inputs in order to:

- Sort the submodule voltages (highest to lowest).
- Allocate switching events to the appropriate submodule, based on the resulting ranking and the current polarity.

Various configurations are possible, offering flexibility on the I/O mapping, selection of the carrier type, or submodule topology (e.g. half- or full-bridge).

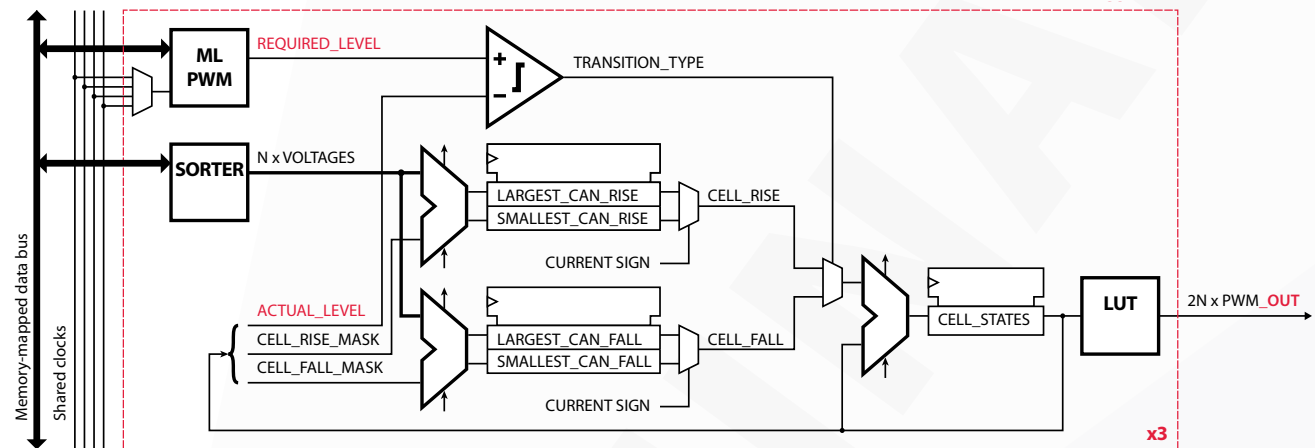


Fig. 40. Internal structure of SS-PWM peripheral blocks.

## USER-PROGRAMMABLE AREA (SANDBOX)

Within its programmable logic area, the B-Box 4 provides a dedicated space for embedding user-defined logic. This provides flexibility for implementing special modulation techniques, or interfacing with external circuits and devices. Within this special area, designated as *sandbox*, two peripheral blocks are pre-implemented for easy-to-use I/O access from/to the CPU cores:

- » **SBI**: Input from the sandbox. This implements read registers that are transferred to the CPU memory simultaneously with other input data (e.g. ADC data).
- » **SBO**: Output to the sandbox. This implements write registers that are transferred from the CPU memory simultaneously with other output data (e.g. PWM data).

Thanks to imperix *RealSync*, these two interfaces are also usable across the control network, which vastly simplifies data access to and from remote FPGAs. The data transfers (read or write) from the CPU are handled by the SBI and SBO blocks either using write-through (configuration) or write-back (real-time) data traffic, as with any other peripheral block. C/C++ drivers and the associated Simulink/PLECS blocks are readily available in the SDKs. For programmable logic developers, templates can be downloaded from the imperix website. Note that other peripheral blocks in the provided HDL source code are obfuscated.

The pre-implemented solution includes a critical optimization: it guarantees that only one submodule switches at any given instant. This minimizes switching losses and optimizes the ratio between the apparent and actual switching frequencies.

| Characteristic                        | Symbol   | Value           |
|---------------------------------------|----------|-----------------|
| Number of submodule per converter arm | N        | 2-24 (-bypass)  |
| Number of output voltage levels       | L        | N+1 or 2N+1     |
| Switching frequency range             | $f_{sw}$ | 3.72 Hz – 1 MHz |
| PWM edge resolution                   |          | 20 ns           |

Table 31. Performance specifications of SS-PWM blocks.

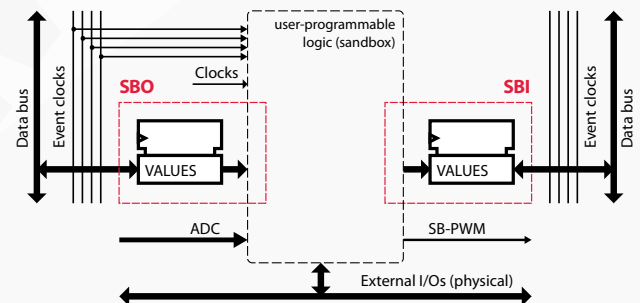


Fig. 41. Internal structure of the SBI and SBO blocks.

The sandbox offers connectivity to the following I/O:

- » ADC values (24x 16 bits signed integers)
- » SB-PWM signals (48 bits register)
- » Internal clocks
- » Physical I/Os (FLT, USR, GPI, GPO)

## SAFETY MECHANISMS

### FAULT MANAGER

At the firmware level, all fault signals are consolidated within the Fault Manager, which oversees the overall system execution state and controls the activation of the PWM outputs. The collected fault signals include:

- **Dedicated fault inputs FLT0..24.** These inputs are shared with GPI pins on the VHDCI connectors A and B. They can be configured from the associated Simulink/PLECS blocks, or the corresponding C++ routine.
- **Analog safety limits on inputs AIN0..24.** These inputs are always active, but can be configured with infinite thresholds when needed. Their configurable thresholds and reaction times can be selected using the front panel or Cockpit.
- **Watchdog counter.** The watchdog is automatically configured with a period of 2.5 times the control processing period. A fault is raised when no data is received by the FPGA within this interval.
- **User faults.** Additional faults can also be declared by software from the user application using the associated Simulink/PLECS block or the corresponding C++ routine.

### HARDWARE MONITORING

The auxiliary safety FPGA present inside the B-Box 4 coordinates the management of faults together with the on-chip fault manager. The collected signals are:

- **Fault flags nFLTx** on VHDCI connectors A, B, C and D. These inputs are active low and are inactive by default. They can be simply left floating when unused.
- **Electrical interlock** at the rear side of the B-Box 4. It operates with 5V logic, and also provide a FAULT status flag as an output for other devices. It can be enabled or disabled using the front panel.
- **Power supplies.** All internal supply voltages are constantly monitored, triggering a fault in case of any malfunction.

### OPERATING STATE MACHINE

The B-Box 4 possesses three possible states of operation:

- **BLOCKED** : The B-Box 4 is running safely but all PWM outputs are currently inhibited for safety purposes (the gate signals are all forced at '0').
- **OPERATING** : The B-Box 4 is running safely. PWM outputs marked as active are effectively produced and delivered to the power stage.
- **FAULT** : A trip condition has been detected, which requires user attention. In this state, all PWM outputs are blocked. Information on the fault source is available in the log (accessible using Cockpit), or through the front panel.

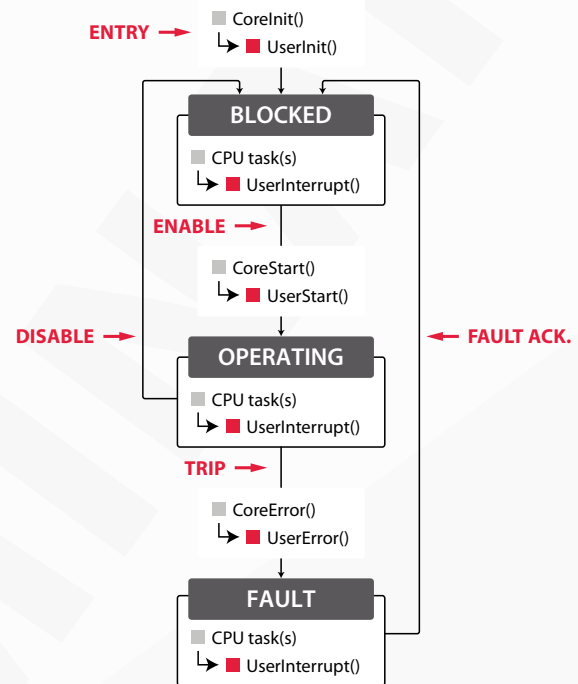


Fig. 42. Flow diagram of the three different states of operation along with their corresponding transitions and trigger events.

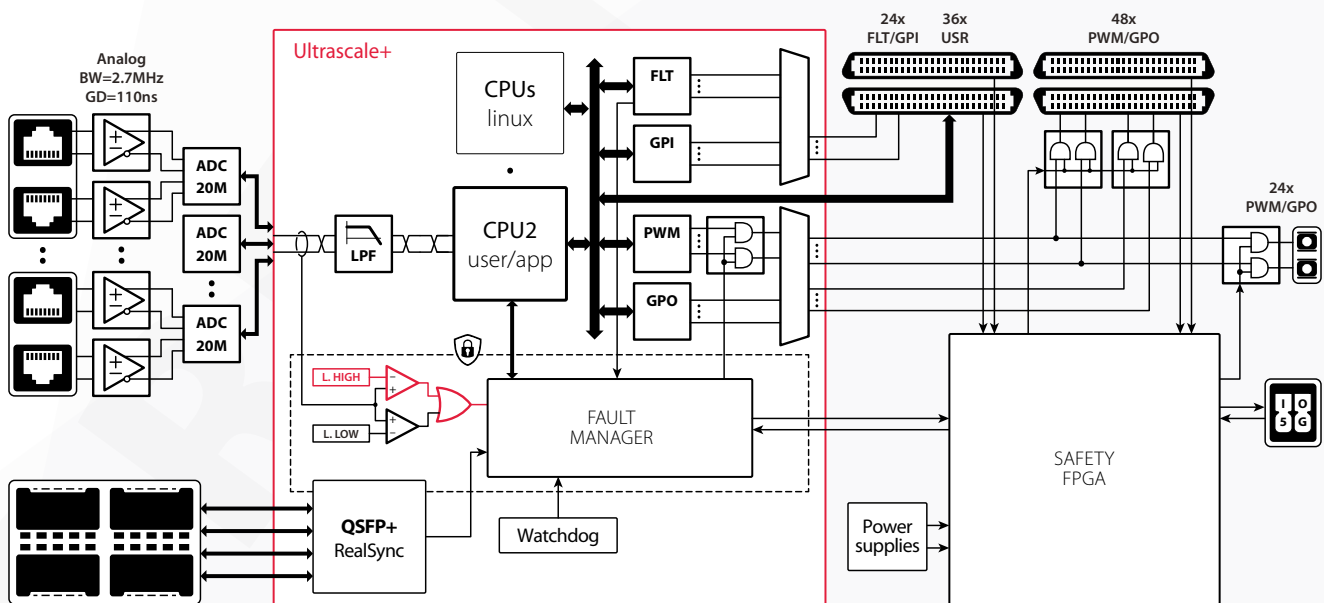


Fig. 43. Internal structure of the FLT peripheral block.

## STATUS LEDs

Three LEDs are present on the front panel of the device to indicate its status.

### POWER LED (PWR)

This LED indicates the power supply's ON/OFF status or any failure or its internal power supplies. Once turned green, it also signals that the device has completed booting.

### SYSTEM LED (SYS)

This LED essentially indicates the operating status of the device with respect to faults. Further information on that topic is given in the "Safety mechanisms" section on page 18. At startup, the LED is also blinking in orange during the synchronization procedure.

### USER LED (USR)

This LED can be freely configured using the Simulink/PLECS blocks, or the corresponding C++ routines.

| LED | Color  | Status         | Information                                    |
|-----|--------|----------------|------------------------------------------------|
| PWR | N/A    | OFF            | Device turned off                              |
|     | Red    | Steady         | Power available                                |
|     | Orange | Steady         | System initializing                            |
|     | Green  | Steady         | System ready                                   |
| SYS | N/A    | OFF            | No code / model running                        |
|     | Red    | Steady         | System in <b>FAULT</b> state (see Fig. 42)     |
|     | Orange | Steady         | System in <b>BLOCKED</b> state (see Fig. 42)   |
|     |        | Blinking – 5Hz | Network synchronization in progress            |
|     | Green  | Steady         | System in <b>OPERATING</b> state (see Fig. 42) |
|     |        | Blinking – 1Hz | Device network ID (at startup)                 |
| USR | Any    | Any            | User-defined behavior                          |

Table 32. Color codes of the status LEDs.

## MECHANICAL DATA

The B-Box 4 is a standard 19"x1U rack-mountable system. It can be mounted within any cabinet using screws up to M6. Its weight is 2.47 kg.

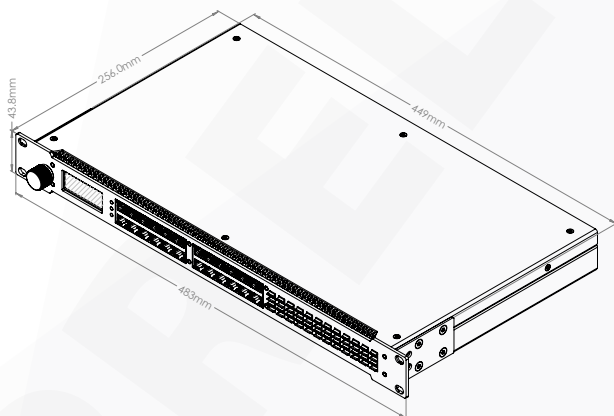


Fig. 44. Mechanical dimensions of B-Box RCP.

## RATED OPERATING CONDITIONS

| Characteristic    | Min. | Typ. | Max. | Unit |
|-------------------|------|------|------|------|
| Input voltage     | 90   |      | 240  | VAC  |
| Power consumption | 5    |      | 60   | W    |
| Inrush current    |      | 95   |      | A    |

Table 33. Rated electrical supply conditions.

| Parameter                               | Value                                                                                                                                                                       |
|-----------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| System voltage                          | 300V, OVC II, PD2                                                                                                                                                           |
| Operating conditions (IEC/EN 60721-3-3) | Climate conditions for operation class 3K3 :<br>– Temperature range: 0°C to +40°C<br>– Relative humidity: < 95%, no condensation<br>– Atmospheric pressure: 70KPa to 106KPa |
| Storage conditions (IEC/EN 60721-3-1)   | Climate conditions for storage class 1K3 :<br>– Temperature range: -25°C to +55°C<br>– Relative humidity: < 95%, no condensation<br>– Atmospheric pressure: 70KPa to 106KPa |
| IP rating                               | IP 20                                                                                                                                                                       |
| Protection class                        | Class I                                                                                                                                                                     |

Table 34. Rated environmental conditions.

## COMPLIANCE STATEMENTS

The B-Box 4 complies with all applicable directives and has been tested according to the associated standards. It meets requirements for emissions in residential environments and susceptibility in industrial environments.

| Characteristic      | Standard        | Conditions      | Result |
|---------------------|-----------------|-----------------|--------|
| ESD                 | IEC 61000-4-2   | IEC 6100-6-2    | pass   |
| Radiated immunity   | IEC 61000-4-3   | IEC 6100-6-2    | pass   |
| Burst immunity      | IEC 61000-4-4   | IEC 6100-6-2    | pass   |
| Surge immunity      | IEC 61000-4-5   | IEC 6100-6-2    | pass   |
| RF CM immunity      | IEC 61000-4-6   | IEC 6100-6-2    | pass   |
| Conducted immunity  | EN 55022/32     | IEC 6100-6-2    | pass   |
| Voltage dips / sags | IEC 61000-4-11  | IEC 6100-6-2    | pass   |
| Conducted emissions | EN 55022/32     | IEC 6100-6-3    | pass   |
| RoHS                | IEC 63000       |                 | pass   |
| Electric safety     | IEC 61010-2-201 | IEC 61010-2-201 | pass   |

Table 35. Electric compliance specifications.

### FCC COMPLIANCE STATEMENT

This device is exempted from compliance with Part 15 of the FCC Rules, pursuant CFR47 §15.103(c) regarding industrial, commercial or medical test equipment.

**CAUTION** Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

### CANADIAN COMPLIANCE STATEMENT

This digital apparatus is exempted from compliance with Canadian ICES-003, pursuant article 1.5.1(d). / Cet appareil numérique est exempté de conformité à la norme NMB-003 du Canada, ainsi que stipulé par l'article 1.5.1(d).

## REVISION HISTORY

• 03.10.25: Preliminary version

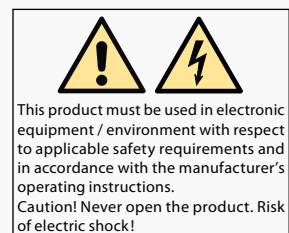
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## ABOUT US

Imperix develops high-end control equipment and prototyping hardware for power electronics, motor drives, smart grids and related topics. Our products are designed to accelerate the implementation of laboratory-scale power converters and facilitate the derivation of high-quality experimental results.



## NOTE

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